Raghul Saravanan

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Education

Ph.D. in Electrical & Computer Engineering **Jan 2023 – Present**
George Mason University, Virginia, USA **GPA: 3.69/4.0**

M.S. in Electrical & Computer Engineering **Aug 2021 – Dec 2023**
George Mason University, Virginia, USA **GPA: 3.61/4.0**

B.Tech. in Electronics and Communications Engineering **Jun 2015 – May 2019**
Amrita Vishwa Vidyapeetham, Coimbatore, India

Professional Experience

George Mason University, Fairfax, Virginia **Jan 2022 – Present**

Graduate Research Assistant *Spring 2023**

- Conducting research on hardware verification, applying coverage-driven and directed fuzzing techniques for automated bug detection in hardware designs.
- Investigating the integration of large language models (LLMs) into electronic design automation (EDA) workflows for hardware design, verification, and security.

Graduate Research Assistant *Summer 2022*

- Designed Reconfigurable Hardware Accelerators for ML Applications using emerging Silicon Nanowire Reconfigurable Field-Effect Transistors (Si-RFETs)

Graduate Teaching Assistant *Spring & Fall 2022*

- Instructor for laboratory sessions in FPGA Design with VHDL and Computer Architecture, guiding students in FPGA prototyping; evaluated assignments and proctored examinations for 100+ students.

9 Corner Solutions, Virginia **May 2026 - Aug 2026**
Hardware Design Research Intern

- Performed design, simulation, synthesis, and automated place-and-route (APR) of digital circuits based on Silicon Nanowire Reconfigurable Field-Effect Transistors (RFETs).

Technische Universität Dresden (TU Dresden), Dresden, Germany **Jun 2023 – Jul 2023**
Visiting Researcher, Supervisor: Dr. Akash Kumar, Chair of Processor Design

- Performed design, simulation, synthesis, and automated place-and-route (APR) of digital circuits based on Silicon Nanowire Reconfigurable Field-Effect Transistors (RFETs).

Semicon, Jaipur, India **Apr 2021 – Jul 2021**
HDL Technical Content Developer

- Authored technical tutorials, articles, and instructional videos on HDL Languages and digital design simulation.

Tekhsol, Coimbatore, India **Mar 2021 – Apr 2021**
Technical Intern

- Designed and developed an Industrial IoT (IIoT) monitoring platform as part of the DevOps team, enabling real-time tracking of assembly line production and machine operations.

Technical Skills

Languages: Verilog, System Verilog, VHDL, Python, C, Tcl, Shell, SQL
Developer Tools: Xilinix Vivado, Synopsys VCS, Synopsys DC, Synopsys TetraMax, Synopsys Library Compiler, Synopsys ICC, Synopsys Verdi, ModelSim, Cadence Xcelium, Cadence Genus, Cadence Conformal, Cadence IMC, Cadence JasperGold, Cadence Innovus, Yosys, ABC
OS: Linux, Windows

Research Projects

Fuzzing Beyond RTL Hardware Designs

- Pioneered coverage-driven fuzzing across multiple abstraction layers of the hardware design flow, extending verification from RTL to gate-level, post-synthesis, and scan-chain designs.
- Developed a suite of fuzzing frameworks—ProFuzz, SynFuzz (post-synthesis gate-level), and TargetFuzz (directed)—each targeting a distinct stage of the design flow.
- Exposed synthesis-introduced and gate-level-only vulnerabilities missed by RTL verification, discovering 4 CVEs and contributing to 1 new CWE.

Fuzzing of Machine Learning Hardware Accelerators

- Hardware fuzzing techniques to ML accelerator designs to uncover functional and security bugs unique to AI hardware.
- Developed targeted input generation strategies tailored to ML hardware architectures, addressing challenges of large state spaces and dataflow-driven control logic.

Redefining Coverage Metrics for Hardware Fuzzing

- Proposed novel coverage metrics at the RTL level to better capture verification completeness in modern hardware fuzzing flows, addressing limitations of traditional RTL code coverage.
- Introduced a cross-layer transaction coverage metric that bridges RTL and gate-level abstractions, enabling unified coverage tracking across the design hierarchy.

Large Language Models (LLMs) for Electronic Design Automation

- Investigating applications of Large Language Models (LLMs) across the EDA flow, including RTL/Verilog code generation, SystemVerilog Assertion (SVA) generation, hardware security analysis, and automated Hardware Trojan insertion.
- Developing agentic LLM frameworks that orchestrate multiple specialized agents to automate RTL to GDSII flow.

Patents and Invention Disclosures

- Sai Manoj P. D., **Raghul Saravanan**, "**Systems and Methods for Hardware Verification**," Application No. 63/794,983, 2024 (Patent Pending).
- Sai Manoj P. D., **Raghul Saravanan**, Jayanth Thangellamudi, Swarup Bhunia, Sudipta Paria, "**HAMMER: Hardware-Aware Mutation Mechanism for Enhanced Hardware Fuzzing**," Application No. 63/938,462, 2025 (Invention Disclosure Filed).

Research Publications

- **Raghul Saravanan**, Sudipta Paria, Sai Manoj P D, Swarup Bhunia, "**Cells of Deception: Generating Stealthy Hardware Trojans using Compromised Library Cells**," IEEE International Conference on Physical Assurance and Inspection of Electronics (PAINE), 2026.
  PDF
- **Raghul Saravanan**, Sudipta Paria, Jayanth Thangellamudi, Swarup Bhunia, Sai Manoj P D, "**Fuzzing Based Verification of Hardware Designs: A Comprehensive Survey**," IEEE Access, 2026.
  ★ Impact Factor: 3.4
  https://ieeexplore.ieee.org/abstract/document/11594832
- Jayanth Thangellamudi, **Raghul Saravanan**, Sai Manoj P D, "**SpecRTL: Specification-Aware Structural Analysis for RTL Using LLM**," 35th IEEE Microelectronics Design & Test Symposium (MDTS), 2026.
  PDF
- **Raghul Saravanan**, Sudipta Paria, Aritra Dasgupta, Swarup Bhunia, P. D. Sai Manoj, "**Intelligent Graybox Fuzzing via ATPG-Guided Seed Generation and Submodule Analysis**," Government Microcircuit Applications & Critical Technology Conference (GOMACTech), 2026.
  https://mason.gmu.edu/~rsaravan/papers/GOMACTech_2026.pdf
- **Raghul Saravanan**, Sai Manoj P D, "**TargetFuzz: Enabling Directed Graybox Fuzzing via SAT-Guided Seed Generation**," 31st Asia and South Pacific Design Automation Conference (ASP-DAC), 2026.
  ✓ Acceptance Rate: 27%
  https://ieeexplore.ieee.org/abstract/document/11420533
- Jayanth Thangellamudi, **Raghul Saravanan**, Sai Manoj P D, "**VeriRAG: A Knowledge Graph-Augmented RAG for Verilog and Assertion Generation**," 31st Asia and South Pacific Design Automation Conference (ASP-DAC), 2026.
  </> https://mason.gmu.edu/~rsaravan/projects/VeriRAG/VeriRAG.html
  ✓ Acceptance Rate: 27%
  https://ieeexplore.ieee.org/abstract/document/11420790

- **Raghul Saravanan**, Sudipta Paria, Swarup Bhunia, Sai Manoj P D, "**PROFUZZ: Directed Graybox Fuzzing via Module Selection and ATPG-Guided Seed Generation**," IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2025.
  </> https://mason.gmu.edu/~rsaravan/projects/profuzz/profuzz.html
  Acceptance Rate: 24%
  https://ieeexplore.ieee.org/abstract/document/11240782

- **Raghul Saravanan**, Sai Manoj P D, "**Exploring Coverage Metrics in Hardware Fuzzing: A Comprehensive Analysis**," ACM Great Lakes Symposium on VLSI (GLSVLSI), 2024.
  Acceptance Rate: 29%
  https://dl.acm.org/doi/abs/10.1145/3649476.3660386

- **Raghul Saravanan**, Sai Manoj P D, "**The Fuzz Odyssey: A Survey on Hardware Fuzzing Frameworks for Hardware Design Verification**," ACM Great Lakes Symposium on VLSI (GLSVLSI), 2024.
  Acceptance Rate: 29%
  https://dl.acm.org/doi/abs/10.1145/3649476.3658697

- **Raghul Saravanan**, Shubham Rai, Akash Kumar, Sai Manoj P D, "**Reconfigurable FET Approximate Computing-based Accelerator for Deep Learning Applications**," IEEE International Symposium on Circuits and Systems (ISCAS), 2023.
  Acceptance Rate: 49.8%
  https://ieeexplore.ieee.org/abstract/document/10181758

- **Raghul Saravanan**, Yaddanapudi Akhileswar, N. Mohankumar, "**N Configuration TRNG Based Scrambler Protocol for Secured File Transfer**," Proceedings of the International Conference on IoT Based Control Networks & Intelligent Systems (ICICNIS), 2021.
  https://papers.ssrn.com/sol3/papers.cfm?abstract_id=3882564

- Yaddanapudi Akhileswar, **Raghul Saravanan**, Chitibomma Meghana, N. Mohankumar, "**Hardware-Assisted QR Code Generation Using Fault-Tolerant TRNG**," International Conference on Communication, Computing and Electronics Systems (ICCCES), Springer, 2020.
  https://link.springer.com/chapter/10.1007/978-981-15-2612-1_19

- S. Bharani Surya, C. Gokul Prasad, **Raghul Saravanan**, N. Mohankumar, "**Evolving Reversible Fault-Tolerant Adder Architectures and Their Power Estimation**," International Conference on Communication, Computing and Electronics Systems (ICCCES), Springer, 2020.
  https://link.springer.com/chapter/10.1007/978-981-15-2612-1_51

- **Raghul Saravanan**, N. Mohankumar, "**Microcontroller Based ANN for Pick and Place Robot Coordinate Monitoring System**," International Conference on Data Science, Machine Learning and Applications (ICDSMLA), Springer, 2020.
  https://link.springer.com/chapter/10.1007/978-981-15-1420-3_35

- Adarsh Krishna, LS Anusree Raj, G. Priyadarsini, **Raghul Saravanan**, S. R. Ramesh, "**A Low Power Binary Square Rooter Using Reversible Logic**," 5th IEEE International Conference on Advanced Computing & Communication Systems (ICACCS), 2019.
  https://ieeexplore.ieee.org/abstract/document/8728490

Presentations and Invited Talks

1. **VeriRAG: A Knowledge Graph-Augmented RAG for Verilog and Assertion Generation**
   January 2026
   IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)
   Hong Kong

2. **TargetFuzz: Enabling Directed Graybox Fuzzing via SAT-Guided Seed Generation**
   January 2026
   IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)
   Hong Kong

3. **Hardware Trojan Detection and Interpretation Using Graph Neural Networks**
   January 2026
   IEEE International Conference on VLSI Design (VLSID)
   Pune, Maharashtra, India

4. **Translation Bugs: Beyond RTL Verification** *(Invited Talk)*
   November 2025
   MITRE RTL Weaknesses Ad-Hoc Working Group
   Virtual

5. **PROFUZZ: Directed Graybox Fuzzing via Module Selection and ATPG-Guided Seed Generation**
   October 2025
   IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
   Munich, Germany

6. **Hardware Fuzzing: A New Frontier in Hardware Security**
   July 2024
   IEEE/ACM Design Automation Conference (DAC)
   San Francisco, California, USA

7. **Exploring Coverage Metrics in Hardware Fuzzing: A Comprehensive Analysis**
   June 2024
   ACM Great Lakes Symposium on VLSI (GLSVLSI)
   Tampa Bay Area, Florida, USA

8. **The Fuzz Odyssey: A Survey on Hardware Fuzzing Frameworks for Hardware Design Verification**
   June 2024
   ACM Great Lakes Symposium on VLSI (GLSVLSI)
   Tampa Bay Area, Florida, USA

9. **Applications of Reconfigurable FETs in Machine Learning Accelerators**
   July 2023
   Guest Scholar Research Seminar, Technische Universität Dresden
   Dresden, Saxony, Germany

10. **Reconfigurable FET Approximate Computing-based Accelerator for Deep Learning Applications**
    May 2023
    IEEE International Symposium on Circuits and Systems (ISCAS)
    Monterey, California, USA

Honors & Awards

HACK@CHES **Fall 2025**

Awarded by Conference on Hardware and Embedded Systems (CHES), Kuala Lumpur, Malaysia

1. Won 2nd place in world's largest hardware hacking competition organized by Intel, Synopsys, Texas A&M, and TU Darmstadt held at CHES, 2026, Kuala Lumpur, Malaysia

HACK@DAC **Summer 2025**

Awarded by Design Automation Conference (DAC), San Francisco, CA

2. Won 1st place in world's largest hardware hacking competition organized by Intel, Synopsys, Texas A&M, and TU Darmstadt held at DAC, San Francisco, California.

Provost Doctoral Fellow Award **Spring 2025**

Awarded by Office of the Provost, George Mason University, Fairfax, Virginia

3. Annual award (AY 2025-2026) recognizing outstanding doctoral students for research excellence, academic achievement, and potential for impactful contributions in their field.

ECE Department Special Recognition Award **Spring 2024**

Awarded by Department of Electrical and Computer Engineering (ECE), GMU, Virginia, USA

4. Annual award to recognize graduate students who have demonstrated outstanding motivation and dedication to the field of study

DAC Young Fellow Award **Spring 2024**

Awarded by Design Automation Conference (DAC), San Francisco, CA

5. Awarded for recognizing promising and early-career researchers with opportunities to attend, learn, and showcase work at the premier DAC conference.

Dr.H.Gilbert Miller Scholarship Award **Fall 2021**

Awarded by College of Engineering and Computing, George Mason University, Virginia, USA

6. Awarded for recognizing outstanding students enrolled in graduate programs

Teaching Experience

Course & Lab Instructor, George Mason University **Spring – Fall 2022**
ECE 445: Computer Organization *Fairfax, Virginia, USA*

Course & Lab Instructor, George Mason University **Spring – Fall 2022**
ECE 448: FPGA Design with VHDL *Fairfax, Virginia, USA*

Mentoring Experience

Raj Balan Palanivel (M.S., Computer Engineering) **Summer 2025**
Research Topic: Agentic AI Workflows for Electronic Design Automation

Soundarya Madhuri Royyuru (M.S., Computer Engineering) **Fall 2024**
Research Topic: Coverage-Guided Fuzzing for RISC-V Processor Verification

Chiranjivan Krishnakumar (M.S., Computer Engineering) **Summer 2024**
Research Topic: Securing Integrated Circuits through Secure EDA and Reverse Engineering Defense

Raja Kumar Janga (M.S., Computer Engineering) **Spring 2024**
Research Topic: Graph Learning for Electronic Design Automation Verification

Charith Sanne (M.S., Computer Engineering) **Spring 2024**
Research Topic: Large Language Models (LLMs) for Hardware Security

Professional Service

Community Service

- Member, MITRE RTL Weaknesses Ad Hoc Working Group.

Technical Program Committees

- TPC Member, IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2024, 2026.
- TPC Member, ACM Great Lakes Symposium on VLSI (GLSVLSI), 2024.

Conference Reviewing

- IEEE International Symposium on Circuits and Systems (ISCAS), 2024, 2025, 2026.
- IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2024, 2026.
- ACM Great Lakes Symposium on VLSI (GLSVLSI), 2024, 2025.
- IEEE International Symposium on VLSI Design and Test (VDAT), 2025.
- IEEE International Conference on Computer Design (ICCD), 2024.

Journal Reviewing

- ACM Transactions on Architecture and Code Optimization (TACO).
- Springer Journal of Hardware and Systems Security.
- International Journal of Reconfigurable and Embedded Systems (IJRES).
- Elsevier Integration, the VLSI Journal.

Selected Media Coverage

HACK@DAC Winners, 2025

- Covered by Intel, DAC, George Mason University News, University of Florida News, 2025.

HACK@CHES, 2025

- Covered by Intel, CHES, George Mason University News, University of Florida News, 2025.