Curriculum Vitae - Rakibul Hassan

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Short Bio: I am working towards a solution for securing embedded systems from the device level to the network level. I have developed solutions for securing integrated chips (ICs) from SAT-based attacks by proposing a Machine Learning-guided Logic-Obfuscation technique, published in several peer-reviewed venues. My current research focuses on Graph-Learning based solutions for detecting Hardware Trojans by analyzing structural features of circuit graphs. I have experience with a variety of Hardware Design and Analysis tools (Synopsys Design Compiler, PrimeTime, VCS, ICC, Xilinx Vivado) and machine learning frameworks (TensorFlow, Keras, DGL). My goal is to integrate problem-solving skills with advanced hardware analysis to design secure hardware systems.

Education

Ph.D. in Electrical and Computer Engineering 2018 – 2023
George Mason University, Fairfax, VA, USA
Supervisor: Sai Manoj Pudukotai Dinakarrao
CGPA: 3.75

B.Sc. in Electrical and Electronic Engineering 2012 – 2016
Ahsanullah University of Science and Technology, Bangladesh
Supervisor: Dr. Satyen Biswas
CGPA: 3.67

Work Experience

Post-Doctoral Associate June 2023 - Present
University of Florida, Gainesville, FL, USA
Research Topics: SoC and SiP security

Graduate Research Assistant May 2019 – May 2023
George Mason University, Fairfax, VA, USA
Research Topics: Trojan Detection, Logic Obfuscation, Malware Epidemic Confinement

Visiting Research Assistant Intern May 2021 - Aug 2021
University of Southern California, Arlington, VA, USA
Research Topics: Graph Learning Based Attack Model for Latch Based Logic Locking

Graduate Teaching Assistant Aug 2018 – May 2019
George Mason University, Fairfax, VA, USA
Courses: VLSI Design for ASICs, Electric Circuit Analysis I

Lecturer (Part-Time) Nov 2017 – Apr 2018
Ahsanullah University of Science and Technology, Dhaka, Bangladesh
Courses: Power Electronics-I Lab

Lecturer Oct 2016 – July 2018
Bangladesh University, Dhaka, Bangladesh
Courses: Electronic Circuit Simulation, Computer Programming Language

Research Interests

- Hardware security and trust
  - System signature analysis of side-channel and malware attacks on multi-core embedded systems
  - Securing hardware against reverse engineering attacks
  - Logic locking and camouflaging techniques
  - Trusted execution environment design and taint tracking techniques
  - Testing and verification of hardware architectures (hardware fuzzing)
- Design and security of IoT networks
  - IoT network security against malware epidemics
  - IoT information propagation and backtracking
  - Zero-trust in IoT networks
  - Energy positive or neutral device authentication in IoT networks

Projects

Hardware Trojan Detection using Graph Neural Network (GNN) May 2021 - Present
- Proposed an IC topology and behavior-aware HT detection approach using structural and behavioral features of the circuit.
- Used gate types, connectivity, operating frequency, and bit-flip patterns under anomalous conditions for HT detection.

Node-level Trust-based Dynamic Distributed Authentication for IoT Networks May 2021 - Present
- Developed an ML-guided Trust-Management model to detect malicious activity on IoT nodes.
- Computed trust scores across nodes based on predicted malicious behavior.

Graph Learning Based Attack Model for Latch Based Logic Locking May 2021 - August 2021
- Developed an ML-based attack model on latch-based logic locking.
- Generated a graph-structured dataset by extracting circuit features and applied graph learning algorithms (DGL).

Malware Epidemic Modeling on IoT Network May 2020 - May 2021
- Proposed a payoff function optimizing network performance and malware propagation on IoT networks.
- Emulated real-world scenarios to develop a malware propagation model using Deter-testbed.

Neural-Network inspired SAT to SAT-Hard Clause Translator May 2019 - Nov 2021
- Developed a neural network-based translator to defend against SAT-based attacks.
- Applied MLP and LSTM for training and integrated the translator block into original circuits.

- Analyzed area and power footprint using hardware design analysis tools.

Teaching Experience

2020 Fall 'VLSI Design for ASICs' (Graduate level course at George Mason Univ.) - *Role:* Teaching Assistant/Grader/Assistant

2020 Spring 'Electric Circuit Analysis I Lab (Lecture 001)' (Bachelors level course at George Mason Univ.) - *Role:* Teaching Assistant

2020 Spring 'Electric Circuit Analysis I Recitation (Lecture 001)' (Bachelors level course at George Mason Univ.) - *Role:* Teaching Assistant

2019 Fall 'Electric Circuit Analysis I Labs (Lecture 001)' (Bachelors level course at George Mason Univ.) - *Role:* Teaching Assistant

2019 Fall 'Electric Circuit Analysis I Recitations (Lecture 001)' (Bachelors level course at George Mason Univ.) - *Role:* Teaching Assistant

2019 Spring 'Electric Circuit Analysis I Labs (Lecture 001)' (Bachelors level course at George Mason Univ.) - *Role:* Teaching Assistant

2019 Spring 'Electric Circuit Analysis I Recitations (Lecture 001)' (Bachelors level course at George Mason Univ.) - *Role:* Teaching Assistant

2018 Fall 'Electric Circuit Analysis I Recitations (Lecture 001)' (Bachelors level course at George Mason Univ.) - *Role:* Teaching Assistant

2018 Spring 'Power Electronics' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2018 Spring 'Computer Programming Language' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2018 Spring 'Power Electronics Lab' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2018 Spring 'Electrical & Electronic Circuits Simulation Lab' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2018 Spring 'Electrical Services Design Lab' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2017 Fall 'Electrical Circuit 2' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2017 Fall 'Electronics 1' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2017 Fall 'Civil Engineering Drawing' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2017 Fall 'Electronic Circuit Simulation' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2017 Fall 'Electrical Service Design' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2017 Fall 'Electrical Properties of Materials' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2017 Spring 'Power Electronics' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2017 Spring 'Power Electronics Lab' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2017 Spring 'Mobile Cellular Communication' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2017 Spring 'Electronic Circuit Simulation Lab' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2017 Spring 'Digital Communication Lab' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2016 Fall 'Power Electronics' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2016 Fall 'Power Electronics Lab' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2016 Fall 'Mobile Cellular Communication' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2016 Fall 'Electronic Circuit Simulation Lab' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

2016 Fall 'Digital Communication Lab' (Undergraduate level course at Bangladesh University) - *Role:* Lecturer

Mentorship

Current PhD Students

Dipayan Saha (University of Florida, Gainesville, USA)

Kawser Bepary (University of Florida, Gainesville, USA)

Pantha Sarker (University of Florida, Gainesville, USA)

Arun Basu (University of Florida, Gainesville, USA)

Henian Li (University of Florida, Gainesville, USA)

Azim Uddin (University of Florida, Gainesville, USA)

Sreenitha Kasarapu (George Mason University, Fairfax, USA)

Raghul Saravanan (George Mason University, Fairfax, USA)

Selected Professional Service

2024	Reviewer for HOST
2023	Reviewer for IEEE TCAD, IEEE Access

Publications

Journals

4. **R. Hassan**, X. Meng, K. Basu, and S. M. P. Dinakarrao, "Circuit Topology-aware Vaccination-based Hardware Trojan Detection," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023.

3. S. Kasarapu, **R. Hassan**, H. Homayoun, and S. M. P. Dinakarrao. "Scalable and Demography-Agnostic Confinement Strategies for COVID-19 Pandemic with Game Theory and Graph Algorithms." COVID vol. 2, no. 6, pp. 767-792, 2022.

2. **R. Hassan**, G. Kolhe, S. Rafatirad, H. Homayoun and S. M. P. Dinakarrao, "A Neural Network-based Cognitive Obfuscation Towards Enhanced Logic Locking," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, doi: 10.1109/TCAD.2021.3138686.

1. M. N. Sakib, **R. Hassan**, S. N. Biswas and S. R. Das, "Memristor-Based High-Speed Memory Cell With Stable Successive Read Operation," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 37, no. 5, pp. 1037-1049, May 2018.

Conferences:

14. **Rakibul Hassan**, Charan Bandi, Meng-Tien Tsai, Shahriar Golchin, S. M. P. Dinakarrao, Setareh Rafatirad, and Soheil Salehi "Automated Supervised Topic Modeling Framework for Hardware Weaknesses," 2023 24th International Symposium on Quality Electronic Design (ISQED), San Francisco, CA, USA, 2023, pp. 1-8.

13. S. Kasarapu, S. Shukla, **R. Hassan**, A. Sasan, H. Homayoun, and S. M. P. Dinakarrao, 2022, June. CAD-FSL: Code-Aware Data Generation based Few-Shot Learning for Efficient Malware Detection. In Proceedings of the Great Lakes Symposium on VLSI 2022, pp. 507-512.

12. **R. Hassan**, S. Rafatirad, H. Homayoun and S. M. P. Dinakarrao, "Performance-aware Malware Epidemic Confinement in Large-Scale IoT Networks," ICC 2021 - IEEE International Conference on Communications, Montreal, QC, Canada, 2021, pp. 1-6.

11. **R. Hassan**, G. Kohle, S. Rafatirad, H. Homayoun and S. M. P. Dinakarrao, "A Cognitive SAT to SAT-Hard Clause Translation-based Logic Obfuscation," 2021 Design, Automation & Test in Europe Conference & Exhibition (DATE), Grenoble, France, 2021, pp. 1172-1177.

10. S. Kasarapu, **R. Hassan**, S. Rafatirad, H. Homayoun and S. M. P. Dinakarrao, "Demography-aware COVID-19 Confinement with Game Theory," 2021 IEEE 3rd International Conference on Artificial Intelligence Circuits and Systems (AICAS), Washington DC, DC, USA, 2021, pp. 1-4.

9. A. Dhavlle, **R. Hassan**, M. Mittapalli and S. M. P. Dinakarrao, "Design of Hardware Trojans and its Impact on CPS Systems: A Comprehensive Survey," 2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea, 2021, pp. 1-5.

8. X. Meng, **R. Hassan**, S. M. P. Dinakrrao and K. Basu, "Can Overclocking Detect Hardware Trojans?," 2021 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, Korea, 2021, pp. 1-5.

7. C. Bandi, S. Salehi, **R. Hassan**, S. M. P. Dinakarrao, H. Homayoun and S. Rafatirad, "Ontology-Driven Framework for Trend Analysis of Vulnerabilities and Impacts in IoT Hardware," 2021 IEEE 15th International Conference on Semantic Computing (ICSC), Laguna Hills, CA, USA, 2021, pp. 211-214.

6. **R. Hassan**, S. Rafatirad, H. Homayoun and S. M. P. Dinakarrao, "Performance-aware Malware Epidemic Confinement in Large-Scale IoT Networks," ICC 2021 - IEEE International Conference on Communications, Montreal, QC, Canada, 2021, pp. 1-6.

5. **R. Hassan**, G. Kolhe, S. Rafatirad, H. Homayoun and S. M. P. Dinakarrao, "SATConda: SAT to SAT-Hard Clause Translator," 2020 21st International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, USA, 2020, pp. 155-160.

4. **R. Hassan**, S. Rafatirad, H. Homayoun and S. M. P. Dinakarrao, "Work-in-Progress: SAT to SAT-Hard Clause Translator," 2019 International Conference on Compliers, Architectures and Synthesis for Embedded Systems (CASES), New York, NY, USA, 2019, pp. 1-2.

3. M. N. Sakib, **R. Hassan** and S. Biswas, "Performance analysis of a memristor-based hybrid memory cell with rapid bidirectional storage capability," 2016 3rd International Conference on Electrical Engineering and Information Communication Technology (ICEEICT), Dhaka, Bangladesh, 2016, pp. 1-6.

2. M. N. Sakib, **R. Hassan** and S. Biswas, "A memristor-based 6T1M hybrid memory cell without state drift during successive read," 2016 9th International Conference on Electrical and Computer Engineering (ICECE), Dhaka, Bangladesh, 2016, pp. 202-205.

1. M. N. Sakib, **R. Hassan** and S. Biswas, "Design a memristor-based hybrid memory cell having faster bidirectional storage operation," 2016 5th International Conference on Informatics, Electronics and Vision (ICIEV), Dhaka, Bangladesh, 2016, pp. 687-692.

References

Ref. 1: Prof. Mark M. Tehranipoor, University of Florida, Gainesville, USA, tehranipoor@ece.ufl.edu
Ref. 2: Prof. Sai Manoj Pudukotai Dinakarrao, George Mason University, USA, spudukot@gmu.edu
Ref. 3: Prof. Brian Mark, George Mason University, USA, bmark@gmu.edu