

# Katayoun Neshatpour

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## EDUCATION

[George Mason University, Fairfax, VA](#)

Ph.D., Computer Engineering, *Expected: Summer 2017*

- Thesis: *Hardware Acceleration of Big Data Applications in MapReduce*
- Advisor: Houman Hodayoun, GPA: 4/4

[Sharif University of Technology, Tehran, Iran](#)

M.Sc., Electronics, Feb 2012

- Thesis: *Design and Implementation of a 4×4 MIMO Detector Applied to the LTE*
- Advisor: Mahdi Shabany

[Isfahan University of Technology, Isfahan, Iran](#)

B.Sc., Electronics, Sep 2009

- Thesis: *Steganography and Steganalysis*
  - Advisor: Saeid Sadri
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## TECHNICAL SKILLS

EDA tools

Xilinx Vivado, Cadence Virtuoso, PSPICE, HSPICE, Codevision, PSIM, NC-Verilog, SOC Encounter, Primetime, Altera Quartus II, Xilinx ISE, ModelSim, Active HDL, SMTSIM, McPAT, Hotspot, Weka

Scripting Language

Python, Perl

HDL Language

Verilog, VHDL

Programming Language

C/C++, MapReduce Hadoop streaming, Pascal, Assembly(C6000 DSP)

Engineering Software

MATLAB, Simulink, Code Composer Studio

Hardware Experience

Xilinx Zedboard and MicroZed featuring Zynq SoC, DE2 and DE2-70 board featuring Altera Cyclone II FPGA, Xilinx Virtex-6 ML605 Evaluation chip, MSP430 microprocessor

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## RESEARCH /WORK EXPERIENCE

- Research on “MapReduce acceleration”. (Spring 2015-present)
  - Microarchitecture analysis on heterogeneous Big+Little Core systems
  - Characterization of Big Data Application on Heterogeneous CPU+FPGA platforms
  - Implementation of machine learning algorithms in Apache Hadoop streaming.
  - Hardware acceleration of the map and reduce functions of MapReduce on Xilinx Zedboard.
- Research on inverse thermal dependence-aware dynamic thermal managements for multi-core processors. (Fall 2014)
- FPGA-optimized adders and modular adders for long integers (Spring 2014)
- A twin axis foam turret with a directional control pad and LCD display controlled by MSP430 microprocessor. (Fall 2013)
- Implementation of the advanced encryption standard (AES) in offset code book mode (OCB), including VHDL and MATLAB implementations. (Fall 2013)
- M.Sc. thesis on “the Design and Implementation of a 4×4 MIMO Detector Applied to the LTE”, including, design, FPGA verification and chip fabrication. (2011-2012)
- Simulation, implementation and verification of several DVB-T digital frontend blocks including Randomizer, inner encoder, Viterbi decoder, Reed Solomon encoder and decoder. (Spring 2010)
- Design, Layout and analysis of a Cascode differential amplifier including DRC, LVS and RC-extracted simulation using Cadence Virtuoso. (Fall 2009)
- B.Sc. thesis on “Steganography and Steganalysis”, including MATLAB implementation of data embedding in picture files, detection and estimation of hidden data using RS Steganalysis. (Summer 2009)

PUBLICATIONS	<b>K. Neshatpour</b> , A. Koohi, H. Homayoun, "Hardware acceleration of biomedical applications in the MapReduce," invited paper in <i>IEEE Int Symp Circuits and Syst</i> , 2015.	ISCAS
	<b>K. Neshatpour</b> , M. Malik, M.A. Ghodrat, S. Avesta, H. Homayoun, "Energy-efficient acceleration of big data analytics applications using FPGAs," in <i>IEEE Big data</i> , 2015.	IEEE Big Data Acceptance rate (17%)
	<b>K. Neshatpour</b> , A. Khajeh, W. Burleson, H. Homayoun, "Revisiting dynamic thermal management exploiting inverse thermal dependence," in <i>proc 25th Great Lakes Symp VLSI</i> , 2015	GLSVLSI Acceptance rate (28%)
	<b>K. Neshatpour</b> , M. Malik, H. Homayoun, "Accelerating machine-learning kernels in Hadoop using FPGAs," <i>15th IEEE/ACM Int Symp Cluster, Cloud and Grid Computing</i> , May 2015.	CCGRID Acceptance rate (25%)
	<b>K. Neshatpour</b> , M. Malik, M.A. Ghodrat, H. Homayoun, "Accelerating Big-Data Analytics Using FPGAs," <i>IEEE 23rd Int Symp Field-Programmable Custom Computing Machines</i> , May 2015.	FCCM
	<b>K. Neshatpour</b> , M. Shabany, P.G. Gulak, "A high-throughput VLSI architecture for a hard and soft SC-FDMA MIMO Detectors," <i>IEEE Trans Circuit and Systems I</i> , pp. 761-770, Feb 2015.	TCAS I
	<b>K. Neshatpour</b> , M. Mahdavi, M. Shabany, "A low-complexity high-throughput ASIC for the SC-FDMA MIMO detectors," in <i>IEEE Int Symp Circuits and Systems</i> , pp. 3065-3068, May 2012	ISCAS
PUBLICATIONS UNDER REVIEW	<b>K. Neshatpour</b> , F. Farahmand, M. Malik, A. Sasan, H. Homayoun, "Hardware accelerated nappers for Hadoop MapReduce streaming," submitted to <i>International Symposium on Computer Architecture</i> , 2016.	ISCA
	M. Malik, <b>K. Neshatpour</b> , H. Homayoun, "Big vs. Little core for energy-efficient Hadoop MapReduce computing," submitted to <i>ACM Sigmetrics</i> , 2015.	Sigmetrics

HONORS AND AWARDS	Travel Awards	<ul style="list-style-type: none"> <li>GSTF travel grant for 2015 IEEE Big Data conference, Santa Clara CA.</li> <li>Student support travel grant to attend ISCAS 2012, Seoul, South Korea.</li> </ul>
	Student Awards	<ul style="list-style-type: none"> <li>George Mason University Summer research assistantship, 2015.</li> <li>George Mason University 3-year presidential scholarship (2013-2016)</li> <li>George Mason University Deans scholarship (2013-2014)</li> </ul>
	Honors	<ul style="list-style-type: none"> <li>Ranked 25<sup>th</sup> among more than 23000 participants in the Master of Electrical Engineering nationwide University Entrance Exam.</li> </ul>

GRADUATE COURSES	Digital Signal Processing Comp Sys performance evaluation Data Convertor CKT design Digital System Design with FPGA	CMOS CKT design Digital Electronics Computer Arithmetic Advanced Microprocessors	Semiconductor Technology ASIC/FPGA sys design Machine Learning
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REFERENCES	Houman Homayoun Assistant Professor George Mason University <a href="mailto:hhomayou@gmu.edu">hhomayou@gmu.edu</a>	Kris Gaj Associate Professor George Mason University <a href="mailto:kgaj@gmu.edu">kgaj@gmu.edu</a>	Mohammad Ali Ghodrat Software Engineer Google Inc <a href="mailto:ghodrat@gmail.com">ghodrat@gmail.com</a>
	Avesta Sasan Researcher Qualcomm <a href="mailto:avesta.sasan@gmail.com">avesta.sasan@gmail.com</a>	Mahdi Shabany Associate Professor Sharif University of Technology <a href="mailto:mahdi@sharif.edu">mahdi@sharif.edu</a>	Wayne Burleson Senior Fellow AMD <a href="mailto:burleson@ecs.umass.edu">burleson@ecs.umass.edu</a>