ASHKAN VAKIL

Ph.D. candidate

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EXECUTIVE SUMMARY

Computer Engineer with experience in Hardware Security, and Physical Design flow of ASIC: Synthesis, PnR, STA, ECO. Interested in PnR, STA, Hardware Trojan detection, and low-power design opportunities.

EDUCATION

May 2021	**Ph.D. Computer Engineering** GPA so far: 4.00/4.00	George Mason University, Fairfax, VA, USA
December 2015	**M.Sc. Electrical Engineering** Overall GPA: 4.00/4.00	University of Bridgeport, Bridgeport, CT, USA
April 2013	**B.S. Electrical Engineering** Overall GPA: 14.63/20.00	University of Mazandaran, Mazandaran, Iran

SKILLS

EDA Tools: Synopsys Design Compiler, Synopsys IC Compiler, Synopsys Primetime, Synopsis Milkyway, Synopsis StarRC, Synopsys HSPICE, Apache RedHawk, Xilinx Vivado, PSPICE, Cadence Genus, Cadence Innovus
Major Python Libraries: Keras, Scikit-learn, Pandas, matplotlib
Programming, Scripting and HDL: Python, Matlab, C/C++, Tcl, VHDL/Verilog

EXPERIENCE

2016 - Present — **George Mason University, Fairfax, VA, USA.**

- Synthesis, Place and Route different IP cores from IWLS and ISCAS benchmarks and run ECO using Synopsys toolset
- Developed a Neural Network model using Keras library to map the delay information of Static Timing Analysis to delay of fabricated IC.
- Developed a Neural Network model using Keras library to map the impact of aging on timing-paths in a semiconductor chip.
- Developed **IR-ATA**, a dynamic scheme to model the voltage variation and jitter noise on the die
- Developed a targeted via stack resizing to mitigate the IR drop on high IR spots in a design
- Developed **LASCA**, a side-channel analysis scheme for hardware Trojan detection, without a Golden IC.
- Implemented TETRIS, the game, on MSP430 microcontroller.
- **Teaching** "Linear Electronics II Lab", "Digital Electronics Lab", "Signals and Systems II" and "Classical Systems and Control Theory" each for 1 semester, and "Electrical Circuit Analysis Lab" for 2 years.

2014 - 2015 — **University of Bridgeport, Bridgeport, CT, USA.**

- Calculated the conductivity of spiral shaped CNT using the Boltzmann transport equation and Schrodinger time-independent equation to mathematically model an energy-harvesting -system using CNT based nantenna.
- **Teaching** "Analog Electronics Lab" and "Modern Electronics" each for 1 year

AWARDS & PUBLICATIONS

- Service Recognition Award from the Great Lakes Symposium on VLSI (GLSVLSI) 2019
- Awarded with Graduate Assistantship (GA) from the University of Bridgeport, for three tandem semesters.
- A Vakil, F Behnia, A Mirzaeian, H Homayoun, N Karimi, A Sasan *"LASCA: Learning Assisted Side Channel Delay Analysis for Hardware Trojan Detection"* ISQED 2020
- A Vakil, H Homayoun, A Sasan, *"IR-ATA: IR Annotated Timing Analysis, A Flow for Closing the Loop Between PDN design, IR Analysis & Timing Closure"* ASP-DAC 2019
- A Vakil, A Alsharani, C Bach, JM Pallis, H Bajwa, *"Fabrication and Mathematical Modeling of SWCNT Scaffold DNA Spiral Nantenna "* *Faculty Research Day, University of Bridgeport,* Connecticut, March 27, 2015
- A. Vakil and H. Bajwa, *"Energy Harvesting Using Graphene Based Antenna for UV Spectrum", Systems, Applications and Technology Conference (LISAT), 2014 IEEE Long Island*, USA, 2 May 2014
- A. Vakil and H. Bajwa, *"Analytical Model of Graphene Based Antenna for Energy Harvesting Applications" Zone 1 Conference for American Society for Engineering Education, University of Bridgeport, Connecticut*, April 3-5, 2014