A Zonotoped Macromodeling for Eye-Diagram Verification of High-Speed I/O Links With Jitter and Parameter Variations

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***Abstract*—It is challenging to efficiently evaluate the performance bound of high-precision analog circuits with input and parameter variations at nano-scale. With the use of zonotope to model uncertainty of input data pattern (or jitter) and multiple parameters, a reachability-based verification is developed in this paper to compute the worst-case eye-diagram. The proposed zonotope-based reachability analysis can consider both spatial and temporal variations in one-time simulation. Moreover, a nonlinear zonotoped macromodeling is further developed to reduce the computational complexity. Performance bound for I/O links considering the parameter variations are evaluated. In addition, the eye-diagrams are generated by the proposed zonotoped macromodel for performance evaluation considering both temporal and spatial variations. As shown by experiments, the zonotoped macromodel achieves up to 450× speedup compared to the Monte Carlo simulation of the original model within small error under specified macromodel order for high-speed I/O links eye-diagram verification.**

***Index Terms*—Eye-diagram verification, I/O links, simulation, variation, zonotoped macromodel.**

I. Introduction

HIGH-SPEED I/O links are critical for high-performance computers by providing an energy-efficient communication between microprocessor cores and memory. Design of Giga-bits/s data-rate I/O links in nano-scale CMOS process is an emerging challenge to handle all kinds of spatial and temporal uncertainties in I/O links under stringent clock rate [1]–[9]. The robust functionality of high-speed links can be assured when they are evaluated by the worst-case eye-diagram under temporal uncertainty or jitter of input data pattern under a desired bit-error-rate (BER). Here, jitter is defined as the temporal deviation in clock signal at one time instant when compared to an ideal clock reference [3], [10]. Majority of the jitter comes from clock generation circuitry such as phase-locked-loop (PLL). It propagates through the communication channel such as high-speed I/O links and can cause data error at the receiver. The conventional evaluation of high-speed I/O links with jitter is to find the worst-case eye-diagram based on tedious Monte Carlo simulations under the desired BER (10^{-12} or less) [11], [12]. It requires a long sequence of the input data pattern that is infeasible for analog verification at advanced technology nodes, which also has large-spatial variations, strong nonlinearities as well as parasitics [13]. In [14], a step response-based eye-diagram prediction is proposed under the step response with only temporal variation.

This paper studies an analog verification problem of high-speed I/O links with temporal and spatial variations. Digital verification [15], [16] can be performed formally with the use of reachability analysis to verify infeasible state from the discretized state space. Recent analog verification [17]–[19] introduces the concept of zonotope that can provide a boundary of multiple state trajectories with time-domain evolution in continuous state space. The zonotope-based reachability analysis has been deployed for a number of hard analog circuit verifications [19]. The work in [20]–[23] further provides a numerical integration as in SPICE to calculate time-evoluted zonotope in state space. As such, one can conveniently have a zonotope-based reachability analysis that provides a predicted performance bound for multiple trajectories under uncertainties from inputs and parameters by one-time computation, in contrast to simulating different trajectories generated one by one in Monte Carlo. The challenge is to further consider parameter variations since the number of locally expanded subspaces by moments can grow substantially [24] when considering all types of parameter variations. However, it is unknown how to formulate a reachability analysis with the consideration of temporal variation of the jitter at input, which is typically required in the analog verification of high-speed I/O links.

Moreover, complexity reduction is not well addressed for the zonotope-based reachability analysis. The calculation of performance bound is expensive with the consideration of multiple parameter variations and jitter variations from input data. Macromodeling via model order reduction (MOR) [25]–[29] can reduce the complexity of state space by subspace-based approximation. The generation of subspace

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can be obtained by Krylov iteration or truncation-balanced realization. However, the effectiveness of subspace generation is limited when considering the strong nonlinearity and parameter variations for analog circuits such as I/Os. In [23] and [30]–[32], parameter variations are included during MOR with the use of interval-values. Correlation-decoupled parameter variations in a statistical range are modeled by interval values. Correlation-decoupled parameter variations in a statistical range are modeled by interval values. However, these works only comprise variations in RLC interconnect, but not applicable to consider uncertainty caused by variation in CMOS transistors. Moreover, it cannot model the temporal variation at input. As a result, I/O circuit uncertainty verification cannot be simulated precisely. In contrast, the proposed work considers variations from both linear devices such as RLC interconnect and nonlinear devices such as CMOS transistors, as well as variations from inputs. The nonlinearity can be addressed during MOR [23], [24], [33]–[35] by constructing a series of local subspaces at different operation points of one trajectory, which can be aggregated to provide one global subspace for approximation. Note that in the previous parameterized nonlinear macromodeling [24], [33]–[35], a weighting sphere is introduced to achieve an approximated subspace based on the neighboring points. The approximation is a weighted combination in which the weights are calculated by Kernel distance. It is not well defined how to build weights in the presence of multiple parameter variations. In contrast, the parameterized subspace is well covered by the zonotope in the proposed method, resulting in a higher accuracy as shown by simulations.

In this paper, a zonotope-based approximation has been applied to describe multiple variations. Temporal variations at input and process variations from circuit parameters are considered in this paper. The temporal variation at input can have significant impact to the jitter; and the parameter process variations can affect the skew. Both can be described by the zonotope-based variation model; and each impact is dependent on the variation strength. Further, reachability analysis is utilized for the analog verification of high-speed I/O links considering the jitter of the input data pattern along with the spatial variation of parameters. To further tackle complexity, a zonotoped macromodel is developed. By constructing local Krylov subspaces in terms of zonotope matrices along the set of trajectories, global subspaces are constructed to approximate the original high-speed I/O links considering both input and parameter variations [24], [35]. Reachability analysis by the order-reduced macromodel is employed to efficiently generate the reachable set as well as the eye-diagram by zonotopes in time-domain without repeated Monte Carlo Simulations. Numerical experiments show that the proposed method achieves up to 450× speedup when compared to Monte Carlo simulation with small error (<6%) under specified macromodel order (order = 7).

The rest of this paper is organized as follows. Section II reviews the high-speed I/O link model and formulates the eye-diagram verification problem. In Section III, zonotope-based reachability analysis is described for the I/O verification under both input and parameter variations. Nonlinear zonotoped macromodeling is further developed in Section IV. Experimental validation results of the proposed method are presented in Section V with the conclusion drawn in Section VI.

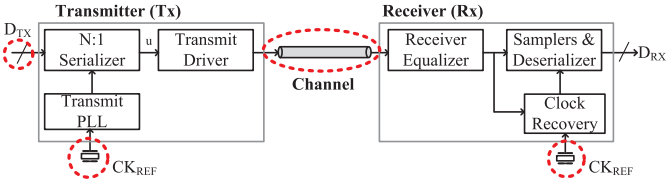

Fig. 1. Simple circuit block diagram of high-speed serial-link I/O transceiver.

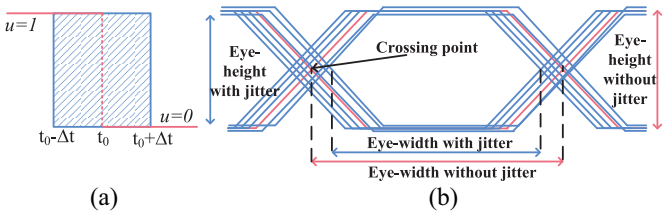

Fig. 2. (a) Temporal variation at input due to jitter. (b) Eye-diagram with and without jitter.

II. I/O Verification Problem

A. Description of I/O Circuit

A basic block diagram of the high-speed serial-link I/O with transceiver is presented in Fig. 1. Transmitter (Tx) circuit consists of serializer (Mux), driver, and PLL. The PLL generates a high-frequency clock, and the serializer multiplexes the input data D_{TX} into a sequence of bits based on the clock frequency. Generated bits are transmitted to receiver through the wired interconnect channel. A chain of inverters, current-mode-logic (CML) or a low-voltage differential signaling buffer can be utilized to transmit the bits generated from the serializer. At the receiver end, receiver consists of three basic blocks, namely an equalizer, a clock recovery, and a data sampler. Based on the clock recovery circuit frequency, samples are collected at the receiver for equalization.

In the high-speed I/O links, slight deviation in the clock frequency due to jitter can introduce serious impact on the data recovery at receiver, which is characterized by an eye-diagram. The major sources of jitter are highlighted by dotted circles in Fig. 1. Considering Fig. 2(b), one can observe the difference in the eye width and height, when there is no jitter (plotted in pink) and when there is jitter (plotted in dark blue). Jitter can introduce significant variation to eye-diagram parameters and introduce error in data recovery with a large BER. This paper focuses on the verification of I/O eye-diagram under jitter and transistor parameter variations. Other external noises can be included similarly.

B. Problem Formulation

Based on the problem description, we formulate an I/O circuit physical verification model considering temporal variation

(or jitter) along with spatial variation of parameters. The input data of I/O circuit with temporal variation (or jitter) shown in Fig. 2(a) can be modeled as follows:

$$u = \begin{cases} 1 & \text{if} \quad t \le t_0 - \Delta t \\ [0,1] & \text{if} \quad t_0 - \Delta t < t \le t_0 + \Delta t \\ 0 & \text{if} \quad t > t_0 + \Delta t \end{cases} \tag{1}$$

where u is the input; Δt represents the jitter; and the shaded region in Fig. 2(a) is the uncertain region, i.e., [0, 1] of the input.

Input jitter can cause a notable BER at the output (receiver). The BER can be approximated from the obtained eye-diagram parameters as follows:

$$\text{BER} = \frac{1}{2}\text{erfc}\left(\frac{\text{Amp(eye)}}{\sqrt{2}\sigma_v}\right). \tag{2}$$

Note that Amp(eye) and σ_v are the eye opening height and the standard deviation of noise at the crossing point of eye, respectively. BER increases with reduction in Width(eye) or increase in noise σ_v. The complementary error function is denoted by erfc().

For a particular design-specified BER, it imposes the width and height requirement of the worst-case eye-diagram by

$$\begin{aligned} \text{Amp(eye)} &\ge A_{\text{th}} \\ \text{Width(eye)} &\ge W_{\text{th}} \end{aligned} \tag{3}$$

where Amp(eye) and Width(eye) are the height and width of the eye respectively. Note that A_{th} and W_{th} indicate the minimum height and width to achieve the desired BER_{th}. As such, the worst-case eye-diagram threshold values need to be calculated for the I/O circuit verification problem defined here.

However, obtaining the worst-case eye-diagram will be time consuming by repeated Monte Carlo simulations due to the long sequence of input data pattern in verification. In this paper, the impact of temporal and spatial variations to I/O circuits is modeled as a bounded polytope of states, called zonotope. Then, the zonotope-based reachability analysis can be developed for the I/O circuit verification. What is more, a zonotoped macromodeling is applied to reduce the complexity with consideration of nonlinearity under variations. Therefore, one-time reachability analysis can be performed efficiently to obtain the worst-case eye-diagram parameters, which are bounded by zonotopes.

III. Zonotoped Reachability Analysis of I/O Verification

In this section, we first discuss some basics of zonotope and modeling of the variations using zonotopes, followed by the reachability analysis for the I/O verification.

A. Basics of Zonotope and its Arithmetic

For better understanding, we review some of the fundamentals of zonotopes for better understanding of rest of this paper.

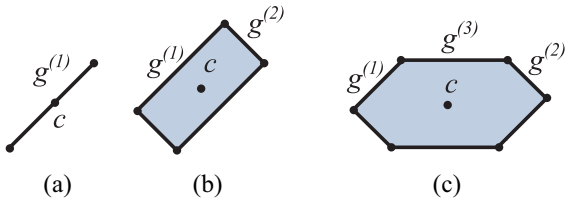

Fig. 3. Construction of zonotope. (a) $c + g^{(1)}$. (b) $c + g^{(1)} + g^{(2)}$. (c) $c + g^{(1)} + g^{(2)} + g^{(3)}$.

Zonotope $\mathcal{Z}$ is a symmetrical type of polytope, mathematically defined as

$$\begin{aligned} \mathcal{Z} &= \left\{ x \in \mathbf{R}^{n\times 1} : x = c + \sum_{i=1}^{q} [-1,1] g^{(i)} \right\} \\ &= \left\{ c, g^{(i)}, g^{(2)}, \ldots \right\} \end{aligned} \tag{4}$$

where $c \in \mathbf{R}^{n\times 1}$ is the zonotope center; q represents number of zonotope generators; and $g^{(i)} \in \mathbf{R}^{n\times 1}$ is a zonotope generator.

As shown in (4), the so-called zonotope is essentially a multidimensional interval in affine form or a hypercube with each generator as a variation in a different direction. Note that ellipsoid-modeled uncertainties are not considered in the reachability analysis in this paper, which will be addressed in future work.

Mathematically, the summation in zonotope needs to be interpreted as the Minkowski summation [18] of two finite sets such that the merged set can preserve convex property. Given two sets of zonotopes P and Q, Minkowski summation is performed by adding their zonotope centers and concatenating their generators as

$$\begin{aligned} P \oplus Q &= \{p + q | p \in P, q \in Q\} \\ &= \left(c_1 + c_2, g_1^{(1)}, \ldots, g_1^{(e)}, g_2^{(1)}, \ldots, g_2^{(u)}\right). \end{aligned} \tag{5}$$

Here, c_1 and c_2 are the centers of zonotopes P, Q, respectively. Generators of P and Q are represented by $g_1^{(i)}$, $g_2^{(i)}$, respectively.

One example of construction of zonotope with the addition of generator vectors is shown in Fig. 3. Here c is the center of zonotope and generator vectors are represented as $g^{(1)}$, $g^{(2)}$, and $g^{(3)}$. The convexity is preserved during the additon of zonotope vectors. In Fig. 3, initially a zonotope with a center c and generator $g^{(1)}$ is presented. Further to perform Minkowski summation, $g^{(2)}$ and its negative vector is added to $g^{(1)}$, which results $g^{(2)}$ in two directions to form a convex zonotope. The same procedure is followed to perform Minkowski summation for additional generators.

B. Modeling Input Variations by Zonotope

The dynamics of a nonlinear system can be expressed by a differential algebraic equation (DAE)

$$\frac{d}{dt} q(x(t)) + f(x(t)) + Bu(t) = 0. \tag{6}$$

Here, $x(t) \in \mathbf{R^n}$ is the state variable vector; $f(x(t))$ includes drain currents of transistor; $q(x(t))$ is the charge accumulated on the gate or parasitic capacitor; B is the incident matrix for current sources and $u(t)$ is the input vector.

For the transient analysis similar as in SPICE, the DAE in (6) can be solved by the linearized multistep integration as

$$C\frac{dx(t)}{dt} + Gx(t) = Bu(t) = b$$
$$C = -\frac{\partial q}{\partial x}|_{x=x^*}, \quad G = -\frac{\partial f}{\partial x}|_{x=x^*}. \tag{7}$$

Here, x^* is the operating point at which the linearization is performed, C is linearized capacitance matrix, G is linearized conductance matrix, and the right hand side vector b contains both the input vector $u(t)$ and the linearization residue of $f(x)$. For the ease of representation, the negative sign is neglected.

Temporal variation or jitter from one input u based on (1) can be written in the form of zonotope by

$$u = \alpha_0 + [-1, 1]\alpha_1. \tag{8}$$

Here, α_0 is the nominal point with jitter modeled by the generator α_1. Similarly, when considering all inputs, an input vector u with jitter can be modeled in the form of a vector zonotope. As an example of three inputs with jitters modeled by (1), one can have

$$u = \begin{pmatrix} u_1 \\ u_2 \\ u_3 \end{pmatrix} = \begin{pmatrix} \alpha_0 \\ \beta_0 \\ \gamma \end{pmatrix} + [-1, 1]\begin{pmatrix} \alpha_1 \\ 0 \\ 0 \end{pmatrix} + [-1, 1]\begin{pmatrix} 0 \\ \beta_1 \\ 0 \end{pmatrix}. \tag{9}$$

Here, u_1, u_2, and u_3 represent three inputs given by $u_1 = \alpha_0 + [-1, 1]\alpha_1$, $u_2 = \beta_0 + [-1, 1]\beta_1$, and $u_3 = \gamma$. Among the three inputs, u_1 and u_2 are expected to have jitter.

C. Modeling Parameter Variations by Zonotope

To model parameter variations, for a linear device like a resistor, the conductance variation $\Delta g^{(i)}$ can be directly expressed in the form of zonotope as

$$g = g_0 + \sum_{i=1}^{q} [-1, 1]\Delta g^{(i)}$$

where g_0 is the nominal value; and q represents number of variations. Whereas for nonlinear devices such as metal-oxide-semiconductor field-effect transistors by Berkeley short-channel IGFET model, the construction of state matrix needs one more step. Suppose that one transistor has a perturbation in width W as ΔW, the variation of its transconductance Δg_m is calculated as

$$\Delta g_m = \frac{\partial g_m}{\partial W}\Delta W. \tag{10}$$

Here, $(\partial g_m/\partial W)$ needs to be computed at one nominal operating point. Other conductances including g_{ds} and g_{mb} can be derived in a similar fashion.

As an example, the generator matrix for inclusion of conductance parameter based on (10) is

$$\Delta G = \begin{pmatrix} \ddots & & \\ & \frac{\partial g_m}{\partial W} & -\frac{\partial g_m}{\partial W} \\ & -\frac{\partial g_m}{\partial W} & \frac{\partial g_m}{\partial W} \\ & & \ddots \end{pmatrix} \Delta W. \tag{11}$$

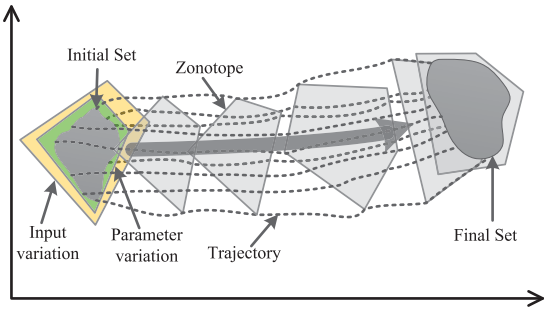

Fig. 4. Reachability analysis in state space with zonotopes for bounded uncertainties.

After the above uncertain system equation is formulated with parameter variations modeled by zonotopes, matrix with multiple-interval-values is given by

$$\mathcal{G} \in \left[\mathcal{G}^{(0)} - \sum_i \left|\Delta\mathcal{G}^{(i)}\right|, \mathcal{G}^{(0)} + \sum_i \left|\Delta\mathcal{G}^{(i)}\right|\right]. \tag{12}$$

Thereby, one can model both input and parameter uncertainties with the use of zonotope.

D. Signal Integrity Analysis via Reachability Analysis

With zonotope to model reachable set under uncertainties, one needs to explore all operating points or states in the state space that an electronic circuit like I/O may visit under variations. As shown in Fig. 4, the time-evolution of zonotopes are calculated as boundary of multiple trajectories, which can be verified (failure or not) when they reach the final set.

Similar to zonotopes, state matrices with uncertain entries can be described in the form of matrix zonotopes as

$$\mathcal{M} = \left\{M \in \mathbf{R}^{n\times n} : M = M^{(0)} + \sum_{i=1}^{q} [-1, 1]M^{(i)}\right\}. \tag{13}$$

Here, $M^{(0)}$ is called the center matrix and the matrix $M^{(i)}$ is called the generator matrix. Additive and multiplication rules for zonotopes and matrix zonotopes are defined in [18]. Note that $M^{(0)}$ can be the linearized state matrix for the nominal operating point; and $M^{(i)}$ contains variations due to multiple parameter variations. Uncorrelated parameter variations after decoupling are filled in different generator matrices.

Once the variations are modeled with the help of (9) and (10), the zonotoped state matrices for G, C, and u can be formed as $\mathcal{G}$, $\mathcal{C}$, and $\mathcal{U}$, respectively. Therefore, the linearized equation in (7) can be formulated with zonotopes and zonotope matrices as

$$\mathcal{C}\frac{d\mathcal{X}(t)}{dt} + \mathcal{G}\mathcal{X}(t) = B\mathcal{U} \tag{14}$$

where $\mathcal{X}$ is the state variable zonotope; $\mathcal{G}$ and $\mathcal{C}$ are the zonotope matrices of G and C with parameter variations; and $\mathcal{U}$ is the zonotope with input variations.

The discretized DAE with zonotopes can be solved by the linear multistep integration such as implicit Euler method [20] with a discretized time-step of h as

$$\mathcal{C}\frac{\mathcal{X}_k - \mathcal{X}_{k-1}}{h} + \mathcal{G}\mathcal{X}_k = B\mathcal{U}. \tag{15}$$

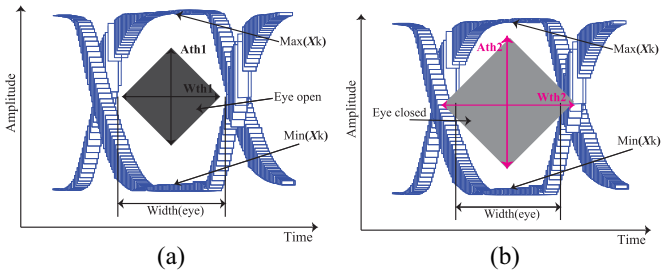

Fig. 5. Eye-diagram verification by zonotope. (a) Eye-open-diagram. (b) Eye-mask-diagram.

As such

$$\mathcal{X}_k = (\mathcal{A})^{-1}\left(\frac{\mathcal{C}\mathcal{X}_{k-1}}{h} + B\mathcal{U}\right) \tag{16}$$

where $\mathcal{A} = ((\mathcal{C}/h) + \mathcal{G})$. It needs to be noted that summation in (16) is performed by Minkowski summation [18]. When there are no input variations, the zonotope $\mathcal{U}$ in (15) and (16) will be normal input vector u. Inverse operation of $\mathcal{A} = (A^{(0)}, \ldots, A^{(q)})$ was not defined in (16), but with approximated LU decomposition to reduce computational complexity [20], which can be implemented in a SPICE-like simulator.

Based on (16), the zonotope of state $\mathcal{X}_k$ at kth time instant can be found. The time-domain eye-diagram thereby will be natively formulated in the final set such that the maximum and minimum values of the zonotope at the final set can be found to calculate the eye opening parameters.

For example, Amp(eye) can be calculated as

$$\text{Amp(eye)} = \max(\mathcal{X}_k) - \min(\mathcal{X}_k).$$

Here, $\min(\mathcal{X}_k)$ and $\max(\mathcal{X}_k)$ are the minimum and maximum values of the zonotope in eye-diagram respectively at the sampling time instant k, as shown in Fig. 5. Similarly, width of the eye-diagram at the crossing point can be calculated as well. As such, one can characterize the worst case eye-opening parameters from the formed zonotope-based reachability analysis for the I/O circuit verification.

Fig. 5 shows the I/O verification using the eye-opening parameters, characterized by the zonotope of final set calculated by (2). When the zonotope of the final set can perfectly embed the specified eye-diagram safety region as described in (3), the according zonotoped eye-diagram of I/O is considered to be open, indicating that the desired BER can be achieved. As shown in Fig. 5(a), the specified eye-diagram with threshold parameters A_{th1} and W_{th1} can be perfectly embedded in the zonotoped eye-diagram. Thus, the eye-diagram is considered to be open and denoted as eye open. Whereas when the zonotope of the final set overlaps over the specified eye-diagram threshold, the according zonotoped eye-diagram of I/O is considered to be closed or failed for the specified BER. If the threshold parameters become A_{th2} and W_{th2}, the zonotoped eye-diagram overlaps with the safety region and hence the eye-diagram is considered to be closed for the specified BER, denoted by eye closed in Fig. 5(b).

Note that compared to the previous symbolic-based bound analysis such as [6], the proposed zonotope-based reachability analysis has two advantages. First, the zonotope-based reachability analysis has well high-order calculation than [6] with full model of transistor for eye-diagram verification in transient domain. The symbolic-based bound analysis [6] can only perform small-signal bound analysis in frequency domain. Second, the zonotope-based reachability analysis can model both temporal input variation (jitter) and also spatial process variation (devices). The symbolic-based bound analysis [6] can only deal with spatial process variation.

IV. Zonotoped Macromodel

To further reduce the complexity of an efficient I/O verification by zonotope-based reachability analysis, the nonlinear macromodeling by MOR can be utilized. In this section, we first show the nonlinear MOR by considering the zonotope-modeled variations from inputs and parameters; and then discuss the reachability analysis under the zonotoped macromodel for I/O verification.

A. Nonlinear Macromodeling

To reduce the computational complexity, a dimension-reduced macromodel can be generated by performing MOR, whereby subspaces are identified to approximate the original full state space.

Suppose a subspace with dimension p is found with $z \in \mathbf{R^p}$ as the reduced state vector, the projection from the original state vector x is expressed by $z = V^T x$. Column vectors in V, $V = [v_1, v_2, \ldots, v_p]$ are the base vectors for the subspace for projection. A nonlinear system with DAE as in (6), the dimension-reduced state vector z satisfies

$$V^T\left[\frac{d}{dt}q(Vz) + f(Vz) + Bu\right] = 0. \tag{17}$$

With the linearization along the trajectory by piece-wise linear approximation at a number of sample points, for example at the jth local sample x_j, the Krylov subspace with an order of p can be constructed as

$$Kr(A_j, r_j, p) = \text{colsp}\left(r_j, A_j r_j, A_j^2 r_j, \ldots, A_j^{p-1} r_j\right) \tag{18}$$

where $A_j = -G_j^{-1}C_j$ and $r_j = -G_j^{-1}b_j$. By orthogonalizing base vectors for Krylov subspace, one can obtain the local subspace for projection matrix V_j. To approximate a nonlinear system, one needs to assemble those V_j together for an aggregated global subspace.

In [35], the subspace of the nonlinear system is constructed by two types of manifolds in the state space. As shown in Fig. 6, by simulating (dc or transient) the full system with the training inputs, a series of sample points are first generated and scattered in the state space as a 1-D manifold, called the dc-manifold. Second, the nonlinear system is linearized and further reduced at each sampled points. The spanned subspace is the so-called ac-manifold.

Suppose a mapping between the jth sample point x_j and one point z_j at the relevant ac-manifold is performed.

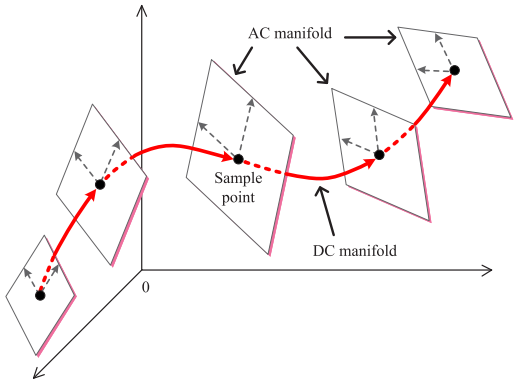

Fig. 6. Manifold-based MOR with dc-manifold and ac-manifold.

For any nearby operating point x, its corresponding mapping point at the relevant ac-manifold is z, can be obtained as

$$\begin{aligned} z &= z_j + V_j^T(x - x_j) \\ x &= x_j + V_j(z - z_j) \end{aligned} \tag{19}$$

and vice-versa for the reverse projection.

As such, the dimension-reduced nonlinear function $f(z)$ becomes

$$\begin{aligned} f(z) &= V_j^T f(x) \\ &= V_j^T\big[f(x_j) + G_j\big(x - x_j\big)\big] \\ &= V_j^T f\big(x_j\big) + V_j^T G_j V_j\big(z - z_j\big). \end{aligned} \tag{20}$$

The same can be derived for the charge function $q(x)$.

Based on (17), the dimension-reduced nonlinear DAE which will be used for simulations can be derived as

$$\frac{dq(z)}{dt} + f(z) + V^T B u = 0. \tag{21}$$

A look-up table is used to store all locally reduced matrices $V_j^T C_j V_j$ and $V_j^T G_j V_j$ [35].

To improve accuracy, neighboring points around one sample point x_i are utilized to approximate $f(z)$ by

$$f(z) = \sum_{i=1}^{k} w_i(z)\Big(V_j^T f(x_i) + V_j^T G_j V_j(z - z_i)\Big).$$

The approximation is a weighted combination, in which the weights $w_i(z)$ are calculated by Kernel distance in a weighting sphere and k denotes number of supported vectors, more details can be found in [36]. However, it is unknown how to build weights to obtain an approximated subspace in the presence of multiple parameter variations with according parameterized subspace.

In the following, we show the nonlinear macromodeling with the use of zonotopes.

B. Zonotoped Macromodel for Variations

As mentioned earlier, it is unknown how to consider variations from multiple parameters as well as input during the nonlinear macromodeling. Individual parameter moment expansion is expensive [24]. With the use of zonotope, zonotope state vector, and zonotope state matrix, the convenient subspace based nonlinear macromodeling with uncertainties can be developed. On the other hand, the zonotope-based reachability analysis would be expensive if the original circuit complexity is high. Therefore, the zonotoped macromodeling is needed for the I/O circuit verification.

The Krylov subspace considering the variation of input and the variation of multiple parameters can be found similar to (18) by replacing the vectors with zonotope matrices as

$$Kr(\mathcal{A}, \mathcal{R}, p) = \text{colsp}\Big(\mathcal{R}, \mathcal{A}\mathcal{R}, \mathcal{A}^2\mathcal{R}, \ldots, \mathcal{A}^{p-1}\mathcal{R}\Big) \tag{22}$$

where $\mathcal{A} = -\mathcal{G}^{-1}\mathcal{C}$ and $\mathcal{R} = -\mathcal{G}^{-1}\mathcal{B}$. As such, the zonotope state vectors form the parameterized Krylov subspace. In our simulations, the maximum number of generators is equal to number of variations.

To orthogonalize the base vectors, QR decomposition needs to be performed. However, $\mathcal{A}^k\mathcal{R}$ of the Krylov subspace cannot be handled directly by the conventional QR decomposition routine. One can first orthogonalize the center matrix

$$Q^{(i)} = M^{(i)}\left(\left(Q^{(0)}\right)^T M^{(0)}\right)^{-1} \tag{23}$$

where the center matrix $M^{(0)}$ is orthogonalized to $Q^{(0)}$, and the zonotope generator matrix $M^{(i)}$ is orthogonalized to $Q^{(i)}$. As such, the orthogonalization of the parameterized subspace $\mathcal{V}$ can be obtained by considering $Q^{(0)}$ as center zonotope and $Q^{(i)}$ as zonotope generator

$$\mathcal{V} = \left\{V \in \mathbf{R}^{n\times n} : V = Q^{(0)} + \sum_{i=1}^{q}[-1, 1]Q^{(i)}\right\}. \tag{24}$$

The construction of the parameterized subspace is performed at each sample point, and is stored to produce the macromodel later.

As a result, one can perform the zonotope-based I/O verification efficiently based on the dimension-reduced macromodel. The state variable z in (21) is now replaced by the zonotope $\mathcal{Z}$ with a nominal center $z^{(0)}$ and a series of generators $z^{(i)}$; and in case of input variations, the input variable u is replaced with zonotope $\mathcal{U}$ with the nominal center α_0 and series of zonotope generators α_i caused by jitters.

The zonotope-based DAE is shown below based on (21) and (24) in the reduced state space

$$\mathcal{V}^T\mathcal{C}\mathcal{V}\frac{d\mathcal{Z}}{dt} + \mathcal{F}(\mathcal{Z}) + \mathcal{V}^T B\mathcal{U} = 0. \tag{25}$$

With the obtained parameterized subspaces at the jth sample point, the projection of $f(x)$ becomes

$$\mathcal{F}(\mathcal{Z}) = \mathcal{V}_j^T f(x_j) + \mathcal{V}_j^T\mathcal{G}_j\mathcal{V}_j\big(\mathcal{Z} - z_j\big). \tag{26}$$

Here, the multiplication of three zonotope matrices is used to evaluate the interval function $\mathcal{F}(\mathcal{Z})$. The sample point x_j in (26) is selected based on the Euclidean distance from the operating point. Recall that the center of zonotope $\mathcal{Z}$ of state vector is used to calculate the Euclidean distance.

Note that the higher-order variation products are discarded as small compared with the first order ones

$$\begin{aligned}\mathcal{V}_j^T\mathcal{G}_j\mathcal{V}_j &= \left(V_j+\Delta V_j\right)^T\left(G_j+\Delta G_j\right)\left(V_j+\Delta V_j\right)\\ &\approx V_j^T G_j V_j + \Delta V_j^T G_j V_j + V_j^T \Delta G_j V_j + V_j^T G_j \Delta V_j\end{aligned} \tag{27}$$

where the variations ΔG_j, ΔV_j refers to the sum of generators in $\mathcal{G}_j$ and $\mathcal{V}_j$.

To solve the zonotope-based DAE in (25), similar to (15), implicit Euler method is applied with discretized time-step h at kth time-step by

$$\mathcal{V}^T\mathcal{C}\mathcal{V}\frac{\mathcal{Z}_k-\mathcal{Z}_{k-1}}{h}+\mathcal{F}(\mathcal{Z}_k)+\mathcal{V}^T B u=0. \tag{28}$$

By substituting $\mathcal{F}(\mathcal{Z}_k)$ with (26), one can obtain

$$\left(\frac{\mathcal{V}^T\mathcal{C}\mathcal{V}}{h}+\mathcal{V}^T\mathcal{G}\mathcal{V}\right)\mathcal{Z}_k=\frac{\mathcal{V}^T\mathcal{C}\mathcal{V}\mathcal{Z}_{k-1}}{h}-\mathcal{V}^T f(x_j) + \mathcal{V}^T\mathcal{G}\mathcal{V}z_j-\mathcal{V}^T B u. \tag{29}$$

Here, $\mathcal{V}$ has the same dimension for all intervals. Performance bound is obtained by transforming the final state set/zonotope into an interval as in (12).

The full multiplication between a zonotope matrix and a zonotope leads to an increased number of generators. The Minkowski summation rule [18] is used to merge zonotopes while preserving new generators created during multiplication

$$\mathcal{Z}_k=\mathcal{A}^{-1}\left(\frac{\mathcal{V}^T\mathcal{C}\mathcal{V}\mathcal{Z}_{k-1}}{h}\oplus -\mathcal{V}^T f(x_j)\oplus\mathcal{V}^T\mathcal{G}\mathcal{V}z_j\oplus -\mathcal{V}^T B\mathcal{U}\right) \tag{30}$$

where $\mathcal{A}=((\mathcal{V}^T\mathcal{C}\mathcal{V})/h)+\mathcal{V}^T\mathcal{G}\mathcal{V}$; and $\oplus$ denotes Minkowski summation. There is a limit on the number of generators in simulation. Only the large generators are preserved after each iteration while the smaller ones are discarded. This can avoid excessive growth of zonotope-matrix size under high accuracy.

The inverse of zonotope matrix $\mathcal{A}=(A^{(0)},\ldots,A^{(i)},\ldots)$ in (30) by the LU decomposition is performed in two-steps. The first step is the approximated expansion of $\mathcal{A}^{-1}$ by

$$\mathcal{A}^{-1}=\left(\left(A^{(0)}\right)^{-1},\ldots,\left(A^{(0)}\right)^{-1}A^{(i)}\left(A^{(0)}\right)^{-1},\ldots\right). \tag{31}$$

The second step is to calculate $(A^{(0)})^{-1}$ by LU decomposition

$$\left(A^{(0)}\right)^{-1}=U^{-1}L^{-1}P^T I \tag{32}$$

where I is the identity matrix and P is the permutation matrix. This approach enables a cost-effective numerical implementation of zonotope-based circuit analysis similar to a SPICE-like simulator.

V. Experimental Results

The proposed zonotope-based I/O eye-diagram verification is implemented in MATLAB on the basis of a SPICE-like simulator. Manipulations of zonotopes are performed by a MATLAB toolbox named Multiparametric Toolbox [37]. Experiment data is collected on a desktop with Intel Core i5 3.2 GHz processor and 8 GB memory.

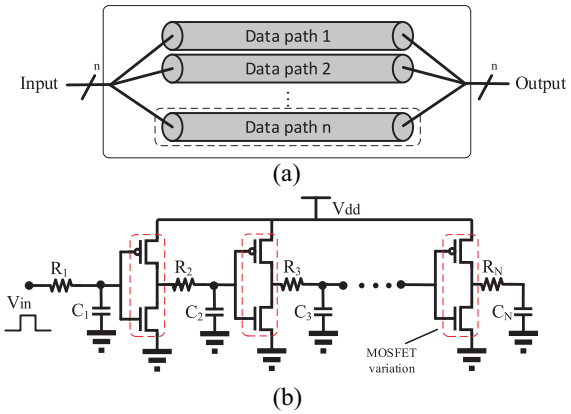

Fig. 7. (a) N-channel inverter-buffer chain with RC-interconnect. (b) Single channel.

CMOS 40 nm technology node is used for the testing I/O circuits: inverter-buffer chain with RC-interconnect and transmission-line (T-line) with CML buffers. The induced variations are randomly introduced. They are simulated with randomly generated input data. In this section, first we show the state space of the I/O circuit considering only spatial variations. The simulations indicate that the zonotope-based reachability analysis can cover most of the uncertainties. Second, we illustrate the eye-diagrams for the I/O links considering the temporal variations as well.

A. Performance Bound Analysis With Only Spatial Variations

Here, we present the performance bound analysis of inverter-buffer chain with RC interconnect and CML buffer with through-silicon interposer I/O realized as T-line considering multiple parameter variations.

1) Inverter-Buffer Chain With RC-Interconnect: The first test-case is a CMOS inverter-buffer chain containing four stages as shown in Fig. 7. Each resistor has an independent variation of 10% (in value); and transistors share a local variation of 5% on their widths. The circuit is simulated for 40 ns with a square-wave signal input active between 5 and 25 ns. The reduced macromodel of the inverter-buffer chain with variations is generated by the proposed zonotoped macromodel. For comparison, the nonlinear MOR [35] is also deployed. The performance bound evaluation by reachability analysis is undertaken afterwards for proposed and nonlinear MOR [35]. To verify the accuracy of reduced macromodels and the Monte Carlo of the full model are performed considering all parameter variations. The performance bound is defined as the spatial variation of voltage-waveform difference (skew) in the state space, where the horizontal axis v_1 represents the voltage on the gate of the third inverter and the vertical axis v_2 is for the voltage on the gate of the fourth inverter.

Performance bound analysis of the reduced macromodels and the Monte Carlo of the full model is shown in Figs. 8 and 9. Proposed and nonlinear MOR [35] are reduced from thirteenth order ($n=13$) to eighth order ($p=8$). In Fig. 8, reachability analysis of the reduced zonotoped macromodel is shown by white blocks with pink envelopes. Each of the blocks is a zonotope for the potential operating points at one time step.

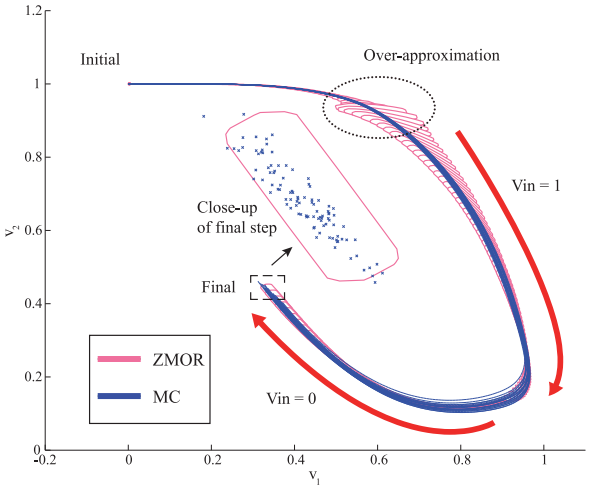

Fig. 8. Performance bound analysis with macromodel by zonotoped-macromodel for a four-stage inverter-buffer chain with RC-interconnect.

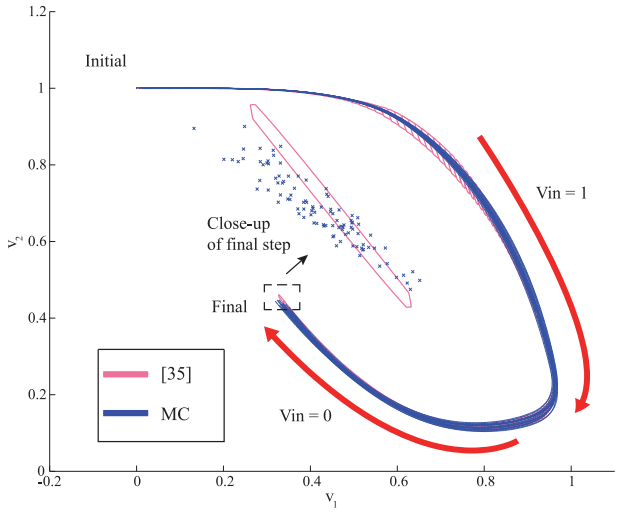

Fig. 9. Performance bound analysis with macromodel by [35] for a four-stage inverter-buffer chain with RC-interconnect.

The blue curves are generated by the Monte Carlo. One can observe that the trajectories move toward the bottom-right corner under the input $V_{\text{in}} = 1$ starting from the top-left corner. After the input signal flips to zero, the trajectories move back toward the initial state. What is more, one can observe that the reduced macromodel with variations manages to fit the trajectories of the full model by the Monte Carlo. There is small error that happens when over-approximation increases as v_1 reaches about 0.6 V. As shown in Fig. 8, more than 90% of the operating points at the final instant by Monte Carlo settle within the final set of reachability analysis based on the proposed model. In contrast, the result of reduced macromodel by [35] is shown in Fig. 9. One can observe that due to the incapability of handling parameter variations, only 40% of operating points of the Monte Carlo at the final time-instant are contained in the final zonotope, which is nearly 50% lower than what is achieved by the proposed model.

Furthermore, the macromodel is obtained with process variation with 15% independent variations of resistors and 10% local variations on transistor widths. Performance summary

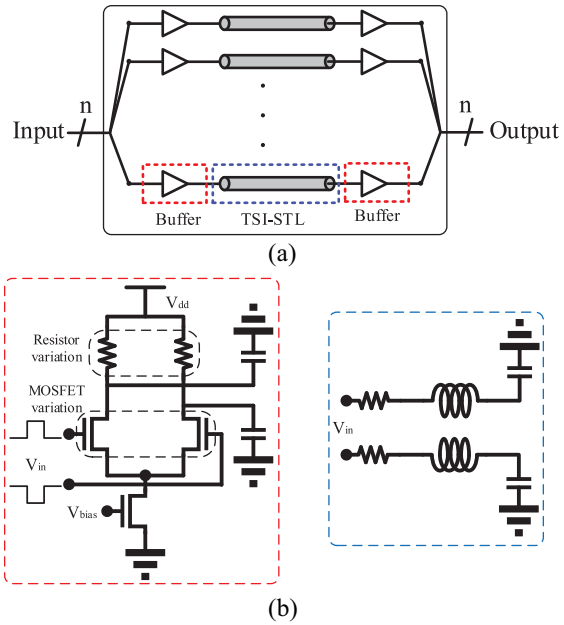

Fig. 10. (a) *N*-channel CML buffer with T-line. (b) Single-channel.

under different conditions is listed in Table I in which the Monte Carlo is performed with 1000 samples, variation gives the variation of local and global parameters and the proposed zonotoped-macromodel refers to the zonotope-based MOR, min and max stand for the lower and upper bounds of the voltage-waveform difference at the final state. One can observe that the difference of the boundaries compared with the Monte Carlo can be limited within 1% for $p = 8$. Up to 500× of speedup can be achieved by the proposed method.

Note that applying MOR can reduce simulation time in two aspects. First, solving matrix takes most of the simulation time and MOR can reduce the size of matrix. Second, the nonlinear circuit is modeled by a series of linearized systems at different operating point. Although the reduced order is not that much high in the inverter-chain experiment, simulation time can be still reduced much when using the MOR macromodel for the nonlinear circuit, instead of running newton iterations on the nonlinear circuits.

Note that the state of final instant to verify in simulation for eye-opening is not a settled state but a transition state.

2) CML Buffer With Transmission Line: Next, we consider a CMOS CML buffer with T-line as shown in Fig. 10. The reduced macromodel with variations is generated by the proposed method with comparison of [35]. The accuracy of the reduced model is validated by comparing with the Monte Carlo of full model considering all parameter variations. Each resistor in the T-line has an independent variation of 10% (in value). The amount of variations in transistor widths are set as 10%. The number of channels can be increased. The performance bound is defined as the spatial variation of voltage-waveform difference (skew) of the CML buffer at different channels.

Performance bound analysis by the reduced macromodels and by the Monte Carlo of full model is shown in Figs. 11 and 12. Both models are reduced from eighteenth order ($n = 18$) to seventh order ($p = 7$). In Fig. 11, reachability analysis by the zonotope macromodel with consideration of

TABLE I
COMPARISON BETWEEN REACHABILITY ANALYSIS OF ZONOTOPED MACROMODEL AND MONTE CARLO FOR A FOUR-STAGE INVERTER-BUFFER CHAIN WITH RC-INTERCONNECT

Test case		ZMOR			Full model MC			Error		Speedup
Variation	Order	Min (V)	Max (V)	Run time (s)	Min (V)	Max (V)	Run time (s)	Min	Max	
5%/10%	$p = 8$	0.4013	0.4616	94.02	0.4008	0.4607	47956.35	0.12%	0.20%	510.1 ×
5%/10%	$p = 7$	0.4243	0.4681	75.49				5.86%	1.61%	635.3×
10%/15%	$p = 8$	0.3721	0.4909	93.89	0.3725	0.4870	47973.11	0.12%	0.80%	511.0×
10%/15%	$p = 7$	0.4033	0.4890	75.21				8.27%	0.41%	637.9×

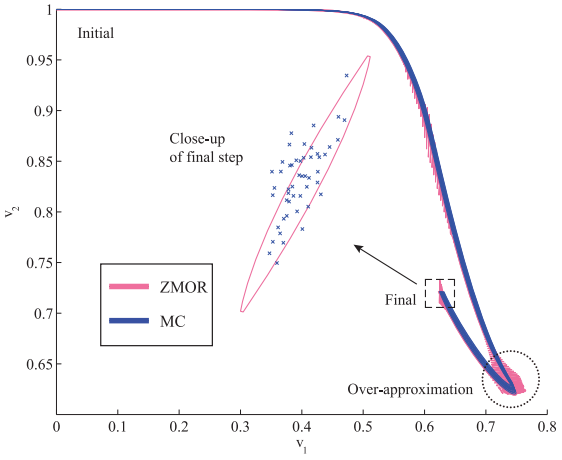

Fig. 11. Performance bound analysis with macromodel by zonotoped-macromodel for CML buffer with T-line.

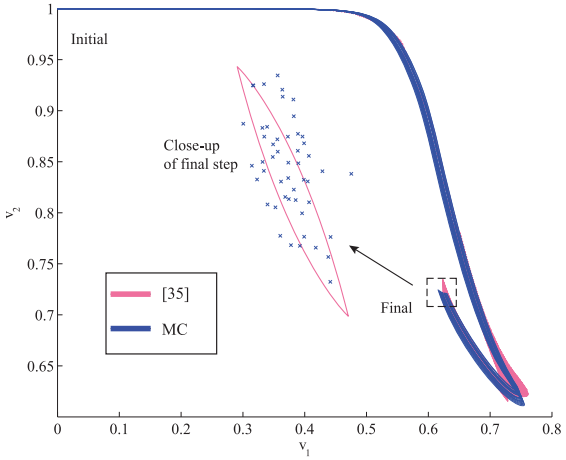

Fig. 12. Performance bound analysis with macromodel by [35] for CML buffer with T-line.

interval-valued parameter variations is shown by white blocks with pink envelope. Each zonotope is a polytope (zoomed-in) that can be clearly observed at the point of over-approximation in the beginning and in the close-up of final state. The blue curves are generated by the Monte Carlo with parameter variations. Over-approximation is observed at the initial points of the trajectory. The proposed method can include the trajectories of the full model within the zonotopes most of the time as shown in Fig. 11. In contrast, as shown in Fig. 12, only 40% of the operating points are included when using the macromodel by [35].

Further, we show performance comparison by increasing the number of channels. Performance summary for different number of channels is listed in Table II in which the Monte Carlo is performed with 1000 samples, ZMOR refers to the reachability-based MOR with zonotope, min and max stand for the lower and upper bounds of the voltage-waveform difference at the final state. Channel represents the number of channels. As shown, the order of reduced model varies with the number of channels. The difference compared to the Monte Carlo can be limited by increasing the order at the cost of extra runtime. For four-channel with reduced order of 10, up to 400× of speedup can be achieved by the proposed method. The difference compared to the Monte Carlo is nearly 3%.

One can observe that with the increase of the original circuit size (36 for two-channel and 72 for four-channel), ZMOR can reduce the order with higher ratio for large-scale circuits to achieve much more speedup but maintains in a lower model order.

B. Eye-Diagram With Spatial and Temporal Variations

Till now, the simulation results considering only spatial, i.e., parameter variations are shown. In this section, we present the eye-diagram verification for the above discussed two test cases considering temporal (jitter) and spatial variations.

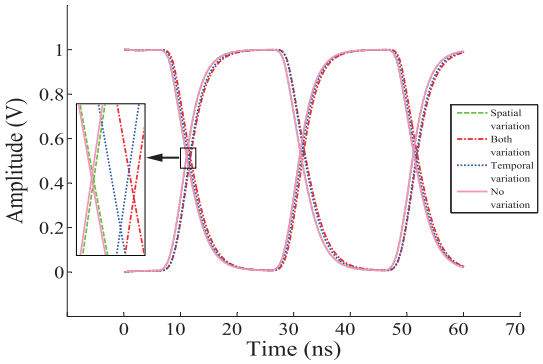

Fig. 13. Impact of spatial and temporal variations for inverter-chain, respectively.

1) Inverter-Buffer Chain With RC-Interconnect: The CMOS inverter-buffer chain in Fig. 7 is considered as I/Os for RC-interconnects. Each resistor has an independent spatial variation of 5% (in value); and transistors share a local spatial variation of 5% on their widths. The inverter chain is simulated with a square-wave of pulse width 20 ns similar to previous test case. Input variations, or jitters, varying from 1% to 10% are experimented. Eye-diagram for the inverter-buffer chain with temporal and spatial variations are generated by the zonotoped macromodel-based reachability analysis in time domain. To further verify the accuracy of the zonotoped macromodel, Monte Carlo simulation of the full model is also performed.

First, we illustrate the impacts on the eye-diagram due to only temporal variation, only spatial variation and their

TABLE II
COMPARISON BETWEEN REACHABILITY ANALYSIS OF ZONOTOPED MACROMODEL AND MONTE CARLO FOR CML BUFFER WITH T-LINE

Test case		ZMOR			Full model MC			Error		Speedup
Channel	Order	Min (V)	Max (V)	Run time (s)	Min (V)	Max (V)	Run time (s)	Min	Max	
1	$p = 7$	0.7037	0.7417	59.94	0.6869	0.7579	20519	2.44%	2.13%	342.3×
2	$p = 9$	0.7052	0.7359	88.32	0.6882	0.7588	33175.26	2.38%	3.01%	375.6×
4	$p = 10$	0.7104	0.7311	194.19	0.6913	0.7543	77267.18	2.76%	3.08%	397.9×

TABLE III
COMPARISON BETWEEN ZONOTOPED MACROMODEL-BASED REACHABILITY ANALYSIS AND MONTE CARLO OF FULL MODEL FOR A FOUR-STAGE INVERTER-BUFFER CHAIN WITH RC-INTERCONNECT

Jitter	Order	Zonotope-based verification			Full model MC			Error		Speedup
		Amp (V)	Width (ns)	Run time (s)	Amp (V)	Width (ns)	Run time (s)	Amp	Width	
1%	p=5	1.0443	18.2	80.18	0.96547	19.5	60342.18	8.17%	6.67%	752.58×
	p=7	0.9539	18.6	132.08				1.19%	4.62%	456.86×
	p=n=13	0.9625	19.1	190.96				0.31%	2.05%	315.99×
10%	p=5	0.9281	13.8	83.62	0.93383	15.9	60066.94	0.61%	13.21%	718.33×
	p=7	0.9313	15.0	134.88				0.27%	5.66%	445.34×
	p=n=13	0.9334	15.1	188.15				0.04%	5.03%	319.25×

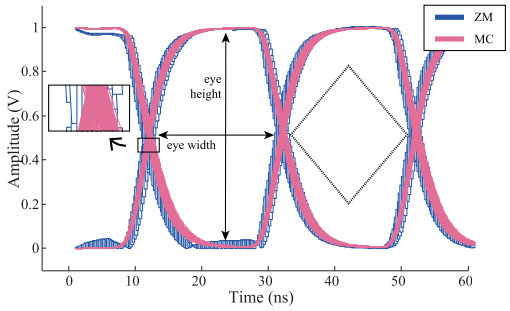

Fig. 14. Zonotope and Monte Carlo-based eye-open-diagrams under 1% jitter for inverter-chain.

combined one. Fig. 13 shows waveforms with individual and combined variations considering input jitter variation of 10%. At one of the output terminals of the inverter chain, one can observe that the waveform (blue) has large displacement (4.5%) of eye width when only temporal variation is present, whereas the waveform (green) by spatial variation has little displacement (1.8%) of eye width. When both temporal and spatial variations are considered together, the waveform (red) has the altered eye width of 7.27%.

Eye-diagrams generated by the proposed zonotoped macromodel and Monte Carlo simulations under a jitter of 1% input variation and 10% spatial variation is shown in Fig. 14. The dark blue curves (MC) are generated by Monte Carlo simulations and white blocks with pink envelope (ZM) are generated by the zonotoped macromodel ($p = 10$). The zonotoped macromodel can fit with the full model ($p = n$) with Monte Carlo by an error of 0.19% in eye-open. The amplitude and width of the eye generated by the zonotoped macromodel as well as the full model are (0.9570 V, 18.9 ns) and (0.9588 V, 19.5 ns), respectively. Both results indicate that the eye-diagram results into the safety region for a BER of 10^{-12} with eye is considered to be open.

In addition, the results for different model orders under different jitters with 5% spatial variations are presented in Table III. Amp and Width indicate the eye height and width, respectively. Monte Carlo simulations are performed with 1000 samples and the corresponding results are presented under full model MC column. Error indicates the difference between the estimated values from the zonotoped macromodel and the full model by Monte Carlo. Note that the eye amplitude obtained from the proposed method is smaller than the Monte Carlo due to over approximation. For a better accuracy macromodel ($p = 7$), nearly 450× speedup is achieved compared to the Monte Carlo simulation. Compared with the zonotope analysis on the original system ($n = 13$), the reduced macromodel can achieve additional 1.45× speedup. The error between the macromodel and Monte Carlo reduces when increasing the order but at the cost of runtime. It needs to be noted that the speedup may be smaller compared to the simulation considering only spatial variations, this is due to increased computations.

In addition, simulation time analysis for zonotoped macromodel of four-stage inverter-buffer chain with 10% jitter is also provided. The simulation time can be divided into three parts: 1) preparation time; 2) MOR time; and 3) transient time. Preparation time comprises of parser and matrix formulation, which is relevant to the circuit size. MOR time and the transient time are relevant to the reduced order. In the simulation, preparation time is 0.11 s for a four-stage inverter-buffer chain for all orders, and the MOR time is 10.51 and 12.94 s for $p = 5$ and 7, respectively. The rest of time is the transient time. Hence one can observe that most of the time is consumed for transient analysis rather than the preparation and MOR time.

2) CML Buffer With Transmission Line: Next, we consider a CMOS CML I/O buffer with T-line interconnect as shown in Fig. 10. Similar to the inverter buffer chain, spatial variations in transistor widths and resistances are set to 5%. The input is a square-wave of pulse width 10 ns with input jitter varied from 1% to 10%. The accuracy and speedup are validated by comparing with the Monte Carlo simulation of the full model.

In Fig. 15, the eye-diagram with 10% jitter of the input by zonotoped macromodel ($p = 12$) is plotted along with the Monte Carlo simulation of the full model. The obtained amplitude and the width of the eye-diagram for the proposed zonotoped macromodel and the full model by the Monte Carlo simulation are (0.6699 V, 7.8 ns) and (0.6761 V, 8.3 ns),

TABLE IV
COMPARISON BETWEEN ZONOTOPED-MACROMODEL-BASED REACHABILITY ANALYSIS AND MONTE CARLO FOR CML BUFFER WITH T-LINE.

Jitter	Order	Zonotope-based verification			Full model MC			Error		Speedup
		Amp (V)	Width (ns)	Run time (s)	Amp (V)	Width (ns)	Run time (s)	Amp	Width	
1%	p=12	0.7313	9.5	111.23	0.7439	9.78	29253.47	1.70%	2.86%	263.00×
	p=n=18	0.7436	9.8	294.65				0.04%	0.20%	99.29×
10%	p=12	0.6699	7.8	110.28	0.6761	8.3	29349.01	0.92%	6.02%	266.13×
	p=n=18	0.6726	8.0	293.61				0.52%	3.61%	99.95×

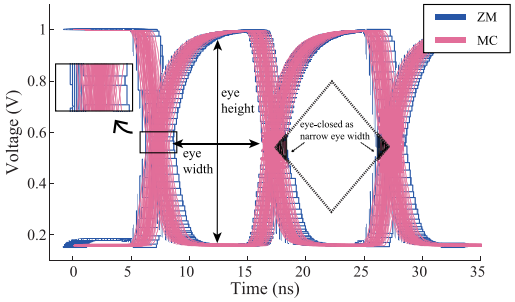

Fig. 15. Zonotope and Monte Carlo-based eye-close-diagrams under 10% jitter for CML-buffer chain.

respectively. The zonotoped macromodel fits the full model Monte Carlo with an error of 0.92% in eye opening. From the zoomed-in figure, one can observe that most of the curves generated by the Monte Carlo of the full model are enclosed within the one by the zonotoped macromodel closely. Note that in contrast to the inverter chain eye-diagram, CML buffer eye-diagram does not reach 0 V due to the presence of the bias.

In addition, the results for the full model and the zonotoped macromodel with different input variations are presented in Table IV. For high accuracy macromodel ($p = 12$) nearly 300× speedup is achieved compared to Monte Carlo simulations with an error less than 1%. Compared with the zonotope analysis on the original system ($n = 18$), the reduced macromodel can achieve additional 2.66× speedup.

For simulation time analysis of CML buffer, preparation time is 0.19 s for all cases, and the MOR time is 12.26 s for $p = 12$. However, one needs to note that with the increase of MOR order, the time increases and transient time also increases.

Lastly, the eye-diagram verification for the case of CML buffer is discussed here based on (2) under the BER of 10^{-12}. Recall that the eye-open condition can be confirmed if the zonotope-formed eye can be embedded into a square of eye-diagram safety region. For the CML buffer with input variations or jitter in Fig. 15, the zonotope-formed eye cannot be embedded into the square of eye-diagram safety region, which indicates that the eye is closed for the given BER under the input variation or jitter with 10% deviation. The verification time is in 110 s.

VI. CONCLUSION

In this paper, a zonotope-based reachability analysis is developed for the verification of high-speed I/O links considering both temporal and spatial variations. The zonotope is introduced to model both jitter and device parameter uncertainty to avoid multiple simulations within long input data sequence for the verification of the worst-case eye-diagram. By zonotope-based reachability analysis, one can generate a set of trajectories with formed performance bound, and each trajectory is associated with a combination of parameter variations. Moreover, nonlinear zonotoped macromodel is further developed to reduce complexity by forming the zonotoped subspace or manifold. As shown by numerical experiments for high-speed I/O links considering temporal and spatial variations, zonotoped macromodel (order = 7) based reachability analysis can generate the worst-case eye-diagram parameters with less than 6% error but with 450× speedup when compared to Monte Carlo simulations of the full model.

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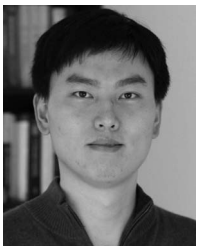

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