A Zonotoped Macromodeling for Reachability Verification of Eye-diagram in High-speed I/O Links with Jitter

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ABSTRACT

With the use of zonotope to model uncertainty of input data pattern (or jitter), a reachability-based verification is developed in this paper to compute the worst-case eye-diagram. The proposed zonotope-based reachability analysis can consider both spatial and temporal variations in one-time simulation of high-speed I/O links. Moreover, nonlinear zonotoped macromodeling is developed to reduce the verification complexity. As shown by experiments, the zonotoped macromodel achieves up to 450× speedup compared to the Monte Carlo simulation of the original model within small error under specified macromodel order for high-speed I/O links verification.

1. INTRODUCTION

High-speed I/O links are critical for high-performance computers by providing energy-efficient communication between microprocessor cores and memory. Design of Giga-bits/s data-rate I/O links in nano-scale CMOS process is an emerging challenge to handle all kinds of spatial and temporal uncertainties in I/O links under stringent clock rate [1, 2, 3]. The robust functionality of high-speed links can be only assured when they are evaluated by the worst-case eye-diagram under temporal uncertainty or jitter of input data pattern under a desired bit-error-rate (BER). Here, jitter is defined as temporal deviation in clock signal at one time instant when compared to an ideal clock reference [1]. Majority of jitter comes from the clock generation circuitry such as PLL. It propagates through the communication channel such as high-speed I/O links and can cause data error at the receiver. The conventional evaluation of high-speed I/O links with jitter is to find the worst-case eye-diagram based on tedious Monte Carlo simulations under the desired BER (10^{-12} or less) [4, 5]. It requires a long sequence of the input data pattern that is infeasible for analog verification at advanced technology nodes, which also has large spatial variations, strong nonlinearities as well as parasitics. In [6], a step response based eye-diagram prediction is proposed under the step response with only temporal variation.

This paper studies an analog verification problem of high-speed I/O links with temporal and spatial variations. Digital verification [7, 8] can be performed formally with the use of reachability analysis to verify infeasible state from discretized state space. The recent analog verification [9, 10, 11] introduces the concept of zonotope that can provide a boundary of multiple state trajectories with time-domain evolution in continuous state space. The work in [12, 13, 14] further provides a numerical integration as in SPICE to calculate time-evolved zonotope in state space. Nonlinearity is addressed by repeated researchable set splitting [12, 13, 14, 15]. As such, one can conveniently have a zonotope-based reachability analysis that provides a predicted performance bound for multiple trajectories under uncertainties from inputs

and parameters by one-time computation, in contrast to simulating different trajectories generated one by one in Monte Carlo. However, it is unknown how to formulate a reachability analysis with consideration of the temporal variation of the jitter at input, which is typically required in the analog verification of high-speed I/O links. Moreover, complexity reduction is not well addressed for the zonotope-based reachability analysis.

In this paper, a zonotope-based reachability analysis is utilized for the analog verification of high-speed I/O links considering the jitter of the input data pattern along with the spatial variation of parameters. The worst-case eye-diagram verification problem can be accordingly formulated by the zonotope-based reachability analysis without repeated Monte Carlo simulations. To further tackle complexity, a zonotoped macromodel is developed. By constructing local Krylov subspaces in terms of zonotope matrices along the set of trajectories, global subspaces are constructed to approximate the original high-speed I/O links considering both input and parameter variations [16, 17]. The reachability analysis by the order-reduced macromodel is employed to efficiently generate the eye-diagram by zonotopes in time-domain. Numerical experiments show that the proposed method achieves up to 450 × speedup when compared to Monte Carlo simulation with small error (<6%) under specified macromodel order (order=7).

The rest of this paper is organized as follows. Section 2 reviews the high-speed I/O link model and formulates the eye-diagram verification problem. In Section 3, zonotope-based reachability analysis is described for the I/O verification under both input and parameter variations. Nonlinear zonotoped macromodeling of I/Os is further developed in Section 4. Experimental validation results of the proposed method are presented in Section 5 with conclusions drawn in Section 6.

2. I/O VERIFICATION PROBLEM
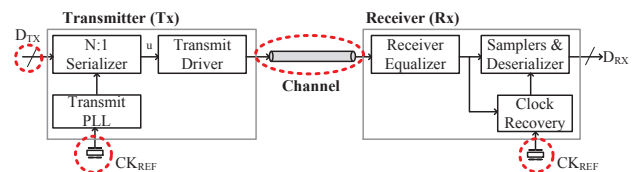
2.1 Description of I/O Circuit

Figure 1: A simple circuit block diagram of high-speed serial-link I/O transceiver

A basic block diagram of the high-speed serial-link I/O transceiver is shown in Fig.1. One can observe that a transmitter (Tx) circuit consists of serializer (Mux), driver and phase-locked-loop (PLL). The PLL generates a high frequency clock. The serializer multiplexes the input data D_{TX} into a sequence of bits based on the clock frequency. Generated bits are are transmitted over the channel to receiver passing the wired interconnect channel. Chain of inverters, current mode logic (CML) or low voltage differential signaling (LVDS) buffer can be utilized to transmit the bits generated from the serializer. At the receiver end, receiver consists

of three basic blocks, namely equalizer, clock recovery and data sampler. Based on the frequency by the clock recovery circuit, sampling is performed at the receiver for equalization.
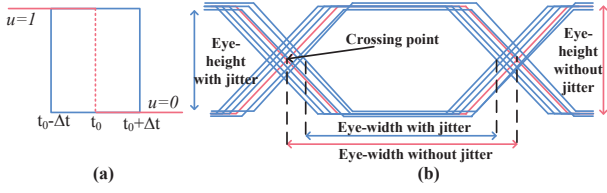

Figure 2: (a) Temporal variation at input due to jitter (b) Eye-diagram with and without jitter

In the high-speed I/O links, slight deviation in the clock frequency due to jitter can introduce serious impact on the data recovery at receiver, which is characterized by an eye-diagram. The major sources of jitter are highlighted by dotted circles in Fig.1. Considering Fig.2(b), one can observe the difference in the eye width and height, when there is no jitter (plotted in pink) and when there is jitter (plotted in dark blue). Jitter can introduce significant variation to eye-diagram parameters and cause error in data recovery with a large bit-error-rate (BER). The scope of this paper studies the verification of I/O eye-diagram under jitter as well as transistor parameter variations. Note that other external noises can be included if needed.

2.2 Problem Formulation

Based on the above problem statement, we formulate a physical verification of the I/O circuit verification problem considering temporal variation (or jitter) along with spatial variation of parameters. The input data of I/O circuit with temporal variation (or jitter) shown in Fig.2(a) can be modeled as follows

$$u = \begin{cases} 1 & if \quad t \le t_0 - \Delta t \\ [0,1] & if \quad t_0 - \Delta t < t \le t_0 + \Delta t \\ 0 & if \quad t > t_0 + \Delta t \end{cases} . \tag{1}$$

where u is the input; Δt represents the jitter; and the shaded region in Fig.2(a) is the uncertain region i.e., $[0,1]$ of the input.

Input jitter can cause a large BER at the output. The BER can be approximated from the obtained eye-diagram parameters as follows

$$BER = \frac{1}{2} erfc(\frac{Amp(eye)}{\sqrt{2}\sigma_v}). \tag{2}$$

Note that σ_v is the standard deviation of the noise at the crossing point of eye: smaller the $Width(eye)$, larger the σ_v and larger the BER; and $erfc$ is the complementary error function.

For a particular design-specified BER_{th}, it imposes the width and height requirement of the worst-case eye-diagram by

$$\begin{aligned} Amp(eye) &\ge A_{th} \\ Width(eye) &\ge W_{th} \end{aligned} \tag{3}$$

where $Amp(eye)$ and $Width(eye)$ are the height and width of the eye-diagram. Note that A_{th} and W_{th} indicate the minimum height and width to achieve the desired BER_{th}. As such, the worst-case eye-diagram threshold values need to be verified for the I/O circuit verification problem defined here.

However, obtaining the worst-case eye-diagram will be time consuming by repeated Monte Carlo simulations due to the long sequence of input data pattern in verification. In this paper, the impact of temporal and spatial variations to I/O circuits is modeled as a bounded polytope of states, called zonotope. Then, the zonotope-based reachability analysis can be developed for the I/O circuit verification. What is more, a zonotoped macromodeling is applied to reduce the complexity with consideration of nonlinearity under variations. As such, one-time reachability analysis can be performed efficiently to obtain the worst-case eye-diagram parameters, which are bounded by the corner of zonotope.

3. ZONOTOPED REACHABILITY ANALYSIS OF I/O VERIFICATION

In this section, we will first discuss how to model the variations in form of zonotopes followed by the reachability analysis for the I/O verification.

3.1 Input and Parameter Variations by Zonotope

Zonotope $\mathcal{Z}$ is a symmetrical type of polytope mathematically defined as:

$$\begin{aligned} \mathcal{Z} &= \{x \in \mathbf{R}^{n \times 1} : x = c + \sum_{i=1}^{q}[-1,1]g^{(i)}\} \\ &= \{c, g^{(i)}, g^{(2)}, ...\} \end{aligned} \tag{4}$$

where $c \in \mathbf{R}^{n \times 1}$ is the zonotope center; q represents number of zonotope generators; and $g^{(i)} \in \mathbf{R}^{n \times 1}$ is a zonotope generator. A zonotope models a reachable set, collection of all operating points or states in the state space that a system may visit under uncertainties from inputs and parameters.

The dynamics of a nonlinear system can be expressed by a differential algebraic equation (DAE)

$$\frac{d}{dt}q(x(t)) + f(x(t)) + Bu(t) = 0. \tag{5}$$

Here, $x(t) \in \mathbf{R^n}$ is the state variable vector; $f(x(t))$ includes drain currents of transistor; $q(x(t))$ is the charge accumulated on the gate or parasitic capacitor; B is the incident matrix for current sources and $u(t)$ is the input vector.

For transient analysis similar as in SPICE, the DAE in (5) can be solved by the multi-step integration with linearization by

$$\begin{aligned} C\frac{dx(t)}{dt} + Gx(t) &= Bu(t) = b \\ C = -\frac{\partial q}{\partial x} \mid_{x=x^*}, \quad G &= -\frac{\partial f}{\partial x} \mid_{x=x^*}. \end{aligned} \tag{6}$$

Here, x^* is the operating point at which the linearization is performed, C is linearized capacitance matrix, G is linearized conductance matrix, and the right hand side vector b contains both the input vector $u(t)$ and the linearization residue of $f(x)$.

Temporal variation or jitter at one input u based on (1) can be written in the form of zonotope by

$$u = \alpha_0 + [-1,1]\alpha_1. \tag{7}$$

Here, α_0 is the nominal point with jitter modeled by the generator α_1. Similarly, when considering all inputs, an input vector u with jitter can be modeled in the form of a vector zonotope. As an example of three inputs with jitters modeled by (1), one can have

$$u = \begin{pmatrix} u_1 \\ u_2 \\ u_3 \end{pmatrix} = \begin{pmatrix} \alpha_0 \\ \beta_0 \\ \gamma \end{pmatrix} + [-1,1] \begin{pmatrix} \alpha_1 \\ 0 \\ 0 \end{pmatrix} + [-1,1] \begin{pmatrix} 0 \\ \beta_1 \\ 0 \end{pmatrix}. \tag{8}$$

Here, u_1, u_2 and u_3 represent 3 inputs with jitters by $u_1 = \alpha_0 + [-1,1]\alpha_1$, $u_2 = \beta_0 + [-1,1]\beta_1$ and $u_3 = \gamma$.

To model parameter variations, for a linear device like resistor, the conductance variation $\Delta g^{(i)}$ can be directly expressed in the form of zonotope as

$$g = g_0 + \sum_{i=1}^{q}[-1,1]\Delta g^{(i)}$$

where g_0 is the nominal value; and q represents number of variations. Whereas for nonlinear devices such as MOSFETs by BSIM models, the construction of state matrix needs one more step. Suppose that one transistor has a perturbation in width W as ΔW, the variation of its transconductance Δg_m is calculated as

$$\Delta g_m = \frac{\partial g_m}{\partial W} \Delta W. \tag{9}$$

Here, $\frac{\partial g_m}{\partial W}$ needs to be computed at one nominal operating point. Other conductances including g_{ds} and g_{mb} can be derived in a similar fashion.

As an example, the generator matrix for inclusion of conductance parameter based on (9) is given below

$$\Delta G = \begin{pmatrix} \ddots & & & \\ & \frac{\partial g_m}{\partial W} & -\frac{\partial g_m}{\partial W} & \\ & -\frac{\partial g_m}{\partial W} & \frac{\partial g_m}{\partial W} & \\ & & & \ddots \end{pmatrix} \Delta W. \quad (10)$$

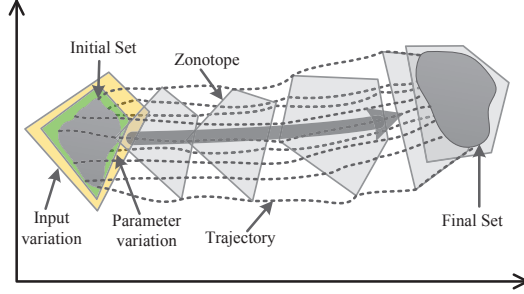Thereby, one can model both input and parameter uncertainties with the use of zonotope.

Figure 3: Reachability analysis in state space with zonotope for bounded uncertainties

3.2 Reachability Analysis of I/O Circuit

With the use of zonotope to model reachable set under all uncertainties, one can explore all operating points or states in the state space that an electronic circuit like I/O may visit under variations. As shown in Fig.3, by modeling the input and parameter variations as zonotopes in initial set, the time-evolution of zonotopes are calculated as boundary of multiple trajectories, which can be verified (failure or not) when they reach the final set.

Similar to zonotopes, state matrices with uncertain entries can be described in the form of *matrix zonotopes* as

$$\mathcal{M} = \{ M \in \mathbf{R}^{n \times n} : M = M^{(0)} + \sum_{i=1}^{q} [-1, 1] M^{(i)} \}. \quad (11)$$

Here, $M^{(0)}$ is called the center matrix and the matrix $M^{(i)}$ is called the *generator matrix*. Additive and multiplication rules for zonotopes and matrix zonotopes are defined in [10]. Note that $M^{(0)}$ can be the linearized state matrix for the nominal operating point; and $M^{(i)}$ contains variations due to multiple parameter variations. Uncorrelated parameter variations after decoupling are filled in different generator matrices.

As such, once the variations are modeled with the help of (8) and (9), the zonotoped state matrices for G, C and u can be formed as $\mathcal{G}$, $\mathcal{C}$ and $\mathcal{U}$, respectively. Therefore, the linearized equation in (6) can be formulated with zonotopes and zonotope matrices as below

$$\mathcal{C} \frac{d\mathcal{X}(t)}{dt} + \mathcal{G}\mathcal{X}(t) = B\mathcal{U} \quad (12)$$

where $\mathcal{X}$ is the state variable zonotope; $\mathcal{G}$ and $\mathcal{C}$ are the zonotope matrices of G and C with parameter variations; and $\mathcal{U}$ is the input zonotope with the input jitter variation, as given in (8).

The discretized DAE with zonotopes can be solved by the linear multi-step integration like implicit Euler method [12] with a discretized time-step of h as

$$\mathcal{C} \frac{\mathcal{X}_k - \mathcal{X}_{k-1}}{h} + \mathcal{G}\mathcal{X}_k = B\mathcal{U}. \quad (13)$$

As such,

$$\mathcal{X}_k = (\mathcal{A})^{-1} (\frac{\mathcal{C}\mathcal{X}_{k-1}}{h} + B\mathcal{U}) \quad (14)$$

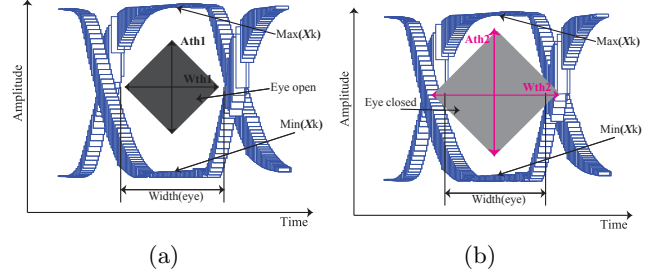(a)   (b)

Figure 4: Eye-diagram verification by zonotope: (a) Eye-open-diagram; (b) Eye-close-diagram

where $\mathcal{A} = (\frac{\mathcal{C}}{h} + \mathcal{G})$. Note that no real inverse of zonotope matrix $\mathcal{A} = (A^{(0)}, ..., A^{(q)})$ in (14) is performed but with approximated LU decomposition to reduce computational complexity [12], similar to a SPICE-like simulator.

Therefore, based on (14), the zonotope of state $\mathcal{X}_k$ at kth time instant can be found. The time-domain eye-diagram thereby will natively formulate in the final set such that the maximum and minimum values of the zonotope at the final set can be found to calculate the eye opening parameters.

For example, $Amp(eye)$ can be calculated as

$$Amp(eye) = max(\mathcal{X}_k) - min(\mathcal{X}_k).$$

Here, $min(\mathcal{X}_k)$ and $max(\mathcal{X}_k)$ are the minimum and maximum values of the zonotope in eye-diagram respectively at the sampling time instant k, as shown in Fig.4. Similarly, width of the eye-diagram at the crossing point can be calculated as well. As such, one can characterize the worst case eye-opening parameters from the formed zonotope-based reachability analysis for the I/O circuit verification.

Fig.4 shows the I/O verification using the eye-opening parameters, characterized by the zonotope of the final set calculated by (2). When the zonotope of the final set can perfectly embed the specified eye-diagram safety region described in (3), the according zonotoped eye-diagram of I/O can be considered to be open, indicating that the desired BER can be achieved. As shown in Fig.4(a), the specified eye-diagram with threshold parameters A_{th1} and W_{th1} can be perfectly embedded in the zonotoped eye-diagram. As such, the eye-diagram is considered to be open and denoted as *Eye open*. Whereas when the zonotope of the final set overlaps over the specified eye-diagram threshold, the according zonotoped eye-diagram of I/O is considered to be closed or failed for the specified BER. If the threshold parameters become A_{th2} and W_{th2}, the zonotoped eye-diagram overlaps with the safety region and hence the eye-diagram is considered to be closed for the specified BER, denoted by *Eye closed* in Fig.4(b).

4. ZONOTOPED MACROMODEL

To further reduce the complexity for an efficient I/O verification by zonotope-based reachability analysis, the nonlinear macromodeling by model order reduction (MOR) can be utilized. In this section, we first show a nonlinear MOR by considering the zonotope-molded variations from inputs and parameters; and then discuss the reachability analysis under the zonotoped macromodel for I/O verification.

4.1 Nonlinear Macromodeling

A dimension-reduced macromodel can be generated by performing MOR to reduce the complexity, whereby subspaces are identified to approximate the original full state space.

Suppose a subspace of dimension p is found with $z \in \mathbf{R^p}$ as the reduced state vector, the projection from the original state vector x is expressed by $z = V^T x$. Column vectors in V, $V = [v_1, v_2, ..., v_p]$ are the base vectors for the subspace for projection. The dimension-reduced state vector z satisfies the dimension-reduced DAE by [18, 17]

$$V^T [\frac{d}{dt} q(Vz) + f(Vz) + Bu] = 0. \quad (15)$$

With the linearization along the trajectory by piece-wise linear approximation at a number of sample points, for example the jth local sample x_j, the subspace V_j is orthogonalized from Krylov subspace obtained below

$$Kr(A_j, r_j, p) = colsp(r_j, A_j r_j, A_j^2 r_j, ..., A_j^{p-1} r_j) \quad (16)$$

where $A_j = -G_j^{-1} C_j$ and $r_j = -G_j^{-1} b_j$.

There is a mapping between the jth sample point x_j and z_j by

$$z = z_j + V_j^T (x - x_j) \quad (17)$$

and vice-versa for the reverse projection. As such, the dimension-reduced nonlinear function $f(z)$ becomes

$$\begin{aligned} f(z) &= V_j^T f(x) \\ &= V_j^T f(x_j) + V_j^T G_j V_j (z - z_j). \end{aligned} \quad (18)$$

The same can be derived for the charge function $q(x)$.

Therefore, the dimension-reduced nonlinear DAE can be derived as

$$\frac{dq(z)}{dt} + f(z) + V^T B u = 0. \quad (19)$$

A look-up table is used to store all locally reduced matrices $V_j^T C_j V_j$ and $V_j^T G_j V_j$ [17].

4.2 Zonotoped Macromodel for Variations

It is unknown how to consider variations from multiple parameter as well as input during the nonlinear macromodeling. Individual parameter moment expansion is expensive [16]. With the use of zonotope, zonotope state vector, and zonotope state matrix, the convenient subspace based nonlinear macromodeling with uncertainties can be developed. On the other hand, the zonotope-based reachability analysis would be expensive if the original circuit complexity is high. Therefore, the zonotoped macromodeling is the need here for the I/O circuit verification.

The Krylov subspace considering the variation of input and the variation of multiple parameters is given as

$$Kr(\mathcal{A}, \mathcal{R}, p) = colsp(\mathcal{R}, \mathcal{A}\mathcal{R}, \mathcal{A}^2 \mathcal{R}, ..., \mathcal{A}^{p-1} \mathcal{R}) \quad (20)$$

where $\mathcal{A} = -\mathcal{G}^{-1}\mathcal{C}$ and $\mathcal{R} = -\mathcal{G}^{-1}\mathcal{B}$. As such, the zonotope state vectors form the parameterized Krylov subspace. Note that the sample point x_j in (24) is selected based on the Euclidean distance from the operating point. The center of zonotope $\mathcal{Z}$ of state vector is used to calculate the Euclidean distance.

To orthogonalize the base vectors, QR decomposition needs to be performed. However, $\mathcal{A}^k \mathcal{R}$ of the Krylov subspace cannot be handled directly by the conventional QR decomposition routine. One can first orthogonalize the center matrix

$$Q^{(i)} = M^{(i)} ((Q^{(0)})^T M^{(0)})^{-1} \quad (21)$$

where the center matrix $M^{(0)}$ is orthogonalized to $Q^{(0)}$, and the zonotope generator matrix $M^{(i)}$ is orthogonalized to $Q^{(i)}$. As such, the orthogonalization of the parameterized subspace $\mathcal{V}$ can be obtained by considering $Q^{(0)}$ as center zonotope and $Q^{(i)}$ as zonotope generator.

$$\mathcal{V} = \{V \in \mathbf{R}^{n \times n} : V = Q^{(0)} + \sum_{i=1}^{q} [-1, 1] Q^{(i)}\}. \quad (22)$$

The construction of the parameterized subspace is performed at each sample point, and is stored to produce the macromodel later.

As a result, one can perform the zonotope-based I/O verification efficiently based on the dimension-reduced macromodel. The state variable z in (19) is now replaced by the zonotope $\mathcal{Z}$ with a nominal center $z^{(0)}$ and a series of generators $z^{(i)}$; and the input variable u is replaced with zonotope $\mathcal{U}$ with the nominal center α_0 and series of zonotope generators α_i caused by jitters.

The zonotope-based DAE is shown below based on (19) and (22) in the reduced state space

$$\mathcal{V}^T \mathcal{C} \mathcal{V} \frac{d\mathcal{Z}}{dt} + \mathcal{F}(\mathcal{Z}) + \mathcal{V}^T B \mathcal{U} = 0. \quad (23)$$

With the obtained parameterized subspaces at the jth sample point, the projection of $f(x)$ becomes

$$\mathcal{F}(\mathcal{Z}) = \mathcal{V}_j^T f(x_j) + \mathcal{V}_j^T \mathcal{G}_j \mathcal{V}_j (\mathcal{Z} - z_j). \quad (24)$$

Here, the multiplication of three zonotope matrices are used to evaluate the interval function $\mathcal{F}(\mathcal{Z})$.

Note that the higher-order variation products are discarded as small compared with the first order ones:

$$\begin{aligned} \mathcal{V}_j^T \mathcal{G}_j \mathcal{V}_j &= (V_j + \Delta V_j)^T (G_j + \Delta G_j)(V_j + \Delta V_j) \\ &\approx V_j^T G_j V_j + \Delta V_j^T G_j V_j + V_j^T \Delta G_j V_j + V_j^T G_j \Delta V_j \end{aligned} \quad (25)$$

where the variations ΔG_j, ΔV_j refer to the sum of generators in $\mathcal{G}_j$ and $\mathcal{V}_j$. The full multiplication between a zonotope matrix and a zonotope leads to an increased number of generators. The Minkowski summation rule [10] is used to merge zonotopes while preserving new generators created during multiplication

$$\mathcal{Z}_k = \mathcal{A}^{-1} \left(\frac{\mathcal{V}^T \mathcal{C} \mathcal{V} \mathcal{Z}_{k-1}}{h} \oplus -\mathcal{V}^T f(x_j) \oplus \mathcal{V}^T \mathcal{G} z_j \oplus -\mathcal{V}^T B \mathcal{U} \right) \quad (26)$$

where $\mathcal{A} = \frac{\mathcal{V}^T \mathcal{C} \mathcal{V}}{h} + \mathcal{V}^T \mathcal{G} \mathcal{V}$; and $\oplus$ denotes Minkowski summation. Here, Minkowski summation of zonotopes P and Q is mathematically defined as

$$\begin{aligned} P \oplus Q &= \{p + q | p \in P, \; q \in Q\} \\ &= (c_1 + c_2, \; g_1^{(1)}, ..., g_1^{(e)}, g_1^{(1)}, ..., g_1^{(e)}) \end{aligned} \quad (27)$$

where c_1 and c_2 represent the centers of zonotopes P, Q respectively, having corresponding generator vectors $g_1^{(i)}$ and $g_2^{(i)}$. As such, Minkowski summation is summation of the zonotope centers and concatenation of their generator vectors.

5. EXPERIMENTAL RESULTS

The proposed zonotope-based I/O eye-diagram verification is implemented in MATLAB on the basis of a SPICE-like simulator. Manipulations of zonotopes are performed by a MATLAB toolbox named Multi-Parametric Toolbox (MPT) [19]. Experiment data is collected on a desktop with Intel Core i5 3.2GHz processor and 8GB memory. CMOS $40nm$ is used as the technology node for the testing I/O circuits: inverter-buffer chain with RC-interconnect and transmission-line (T-line) with current-mode-logic (CML) buffers. The induced variations are randomly introduced. They are simulated with input signal bit-stream of 400-bit randomly generated to consider input variations. Other patterns can be considered similarly.

5.1 Inverter-buffer Chain with RC-interconnect

The CMOS inverter-buffer chain in Fig.5 is considered as I/Os for RC-interconnects. Each resistor has an independent spatial variation of 5% (in value); and transistors share a local spatial variation of 5% on their widths. The inverter chain is simulated with a square-wave of pulse width $20ns$. Input variations, or jitters, varying from 1% to 10% are experimented. Eye-diagrams for the inverter-buffer chain with temporal and spatial variations are generated by the zonotoped-macromodel based reachability analysis in time domain. To further verify the accuracy of the zonotoped macromodel, Monte Carlo simulation of the full model is also performed.

First, we illustrate the impacts on the eye-diagram due to only temporal variation, only spatial variation and their combined one. Fig.6 shows waveforms with individual and combined variations considering input jitter variation of 10%. At one terminal of outputs of the inverter chain, one can observe that the waveform (blue) has large displacement (4.5%) of eye width when only

Table 1: Comparison between zonotoped-macromodel based reachability analysis and Monte Carlo of full model for a 4-stage inverter-buffer chain with RC-interconnect

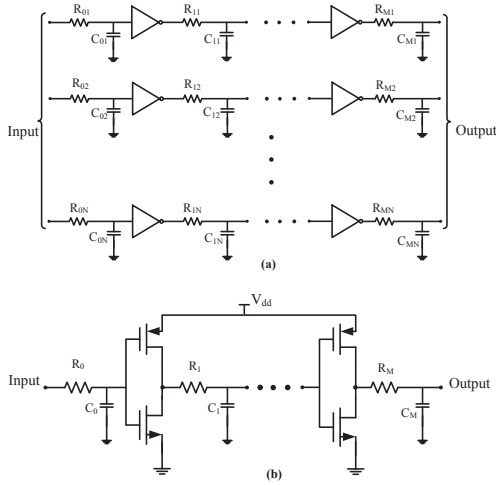| Jitter	Order	Zonotope-based verification			Full model MC			error		speedup
		Amp (V)	Width (ns)	run time (s)	Amp (V)	Width (ns)	run time (s)	Amp	Width	
1%	p=5	1.0443	18.2	80.18	0.96547	19.5	60342.18	8.17%	6.67%	752.58×
	p=7	0.9539	18.6	132.08				1.19%	4.62%	456.86×
	p=n=13	0.9625	19.1	190.96				0.31%	2.05%	315.99×
10%	p=5	0.9281	13.8	83.62	0.93383	15.9	60066.94	0.61%	13.21%	718.33×
	p=7	0.9313	15.0	134.88				0.27%	5.66%	445.34×
	p=n=13	0.9334	15.1	188.15				0.04%	5.03%	319.25×

Figure 5: Inverter-buffer chain with RC-interconnect: (a) N-channel; (b) Single channel
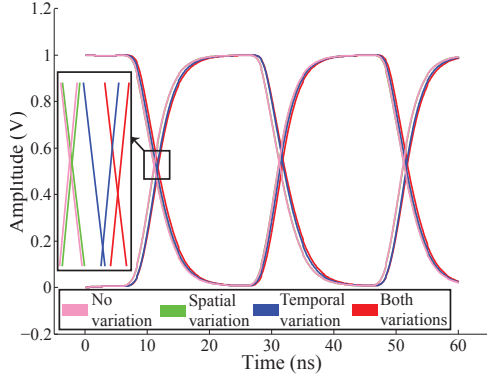

Figure 6: Impact of spatial and temporal variations for inverter-chain respectively

Figure 7: Zonotope and Monte Carlo based eye-open-diagrams under 1% jitter for inverter-chain

column. *Error* indicates the difference between the estimated values from the zonotoped macromodel and the full model by Monte Carlo. Note that the eye amplitude obtained from the proposed method is smaller than the Monte Carlo due to over approximation. For a high accuracy macromodel ($p = 7$), nearly $450\times$ speedup is achieved compared to the Monte Carlo simulation. The error between the macromodel and Monte Carlo reduces when increasing the order but at the cost of runtime.

5.2 CML Buffer with Transmission Line
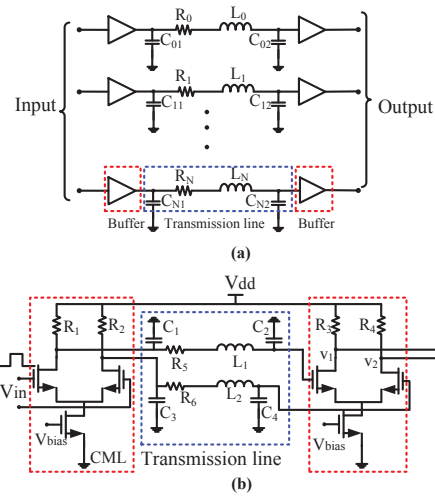
Figure 8: CML-buffer chain with transmission line:(a) N-channel; (b) Single-channel

Next, we consider a CMOS current-mode-logic (CML) I/O buffer with transmission line (T-line) interconnect as shown in Fig.8. Similar to the inverter buffer chain, spatial variations in transistor widths and resistances are set to 5%. The input is a square-wave of pulse width $10ns$ with input jitter varied from 1% to 10%. The accuracy and speedup are validated by comparing with the Monte Carlo simulation of the full model.

In Fig.9, the eye-diagram with 10% jitter of the input by zonotoped-macromodel (order $p = 12$) is plotted along with the Monte Carlo simulation of the full model. The obtained amplitude and

temporal variation is present, whereas the waveform (green) by spatial variation has little displacement (1.8%) of eye width. When both the temporal and spatial variations are considered together, the waveform (red) has the altered eye width of 7.27%.

Eye-diagrams generated by the proposed zonotoped macromodel and Monte Carlo simulations under a jitter of 1% input variation and 10% spatial variation is shown in Fig.7. The dark blue curves (MC) are generated by Monte Carlo simulations and white blocks with pink envelope (ZM) are generated by the zonotoped macromodel (order $p = 10$). The zonotoped macromodel can fit with the full model ($p = n$) with Monte Carlo by an error of 0.19% in eye-open. The amplitude and width of the eye generated by the zonotoped macromodel as well as the full model are $(0.9570V, 18.9ns)$ and $(0.9588V, 19.5ns)$, respectively. Both results indicate that the eye-diagram results into the safety region for a BER of 10^{-12} with eye is considered to be open.

In addition, the results for different model orders under different jitters with 5% spatial variations are presented in Table 1. *Amp* and *Width* indicate the eye height and width, respectively. Monte Carlo simulations are performed with 1000 samples and the corresponding results are presented under *Full model MC*
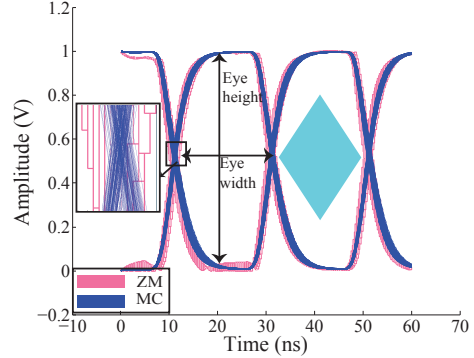
Table 2: Comparison between zonotoped-macromodel based reachability analysis and Monte Carlo for CML buffer with transmission line

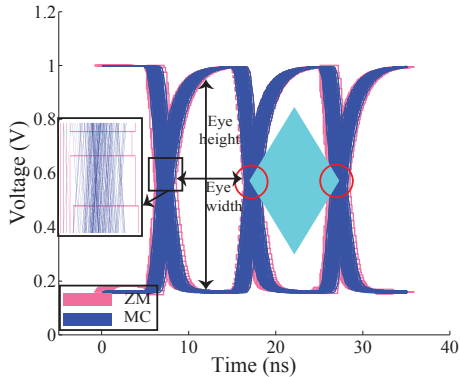| Jitter	Order	Zonotope-based verification			Full model MC			error		speedup
		Amp (V)	Width (ns)	run time (s)	Amp (V)	Width (ns)	run time (s)	Amp	Width	
1%	p=12	0.7313	9.5	111.23	0.7439	9.78	29253.47	1.70%	2.86%	263.00×
	p=n=18	0.7436	9.8	294.65				0.04%	0.20%	99.29×
10%	p=12	0.6699	7.8	110.28	0.6761	8.3	29349.01	0.92%	6.02%	266.13×
	p=n=18	0.6726	8.0	293.61				0.52%	3.61%	99.95×

Figure 9: Zonotope and Monte Carlo based eye-close-diagrams under 10% jitter for CML-buffer chain

the width of the eye-diagram for the proposed zonotoped macro-model and the full model by the Monte Carlo simulation are $(0.6699V, 7.8ns)$ and $(0.6761V, 8.3ns)$, respectively. The zono-toped macromodel fits the full model Monte Carlo with an error of 0.92% in eye opening. From the zoomed-in figure, one can observe that most of the curves generated by the Monte Carlo of the full model are enclosed within the one by the zonotoped macromodel closely. Note that in contrast to the inverter chain eye-diagram, CML buffer eye-diagram does not reach $0V$ due to the presence of the bias.

In addition, the results for the full model and the zonotoped macromodel with different input variations are presented in Table 2. For high accuracy macromodel ($p = 12$) nearly 300× speedup is achieved compared to Monte Carlo simulations with an error less than 1%.

Lastly, the eye-diagram verification for the case of CML buffer is discussed here based on (2) under the BER of 10^{-12}. Recall that the eye-open condition can be confirmed if the zonotope-formed eye can be embedded into a square of eye-diagram safety region. For the CML buffer with input variations or jitter in Fig.9, the zonotope-formed eye cannot be embedded into the square of eye-diagram safety region, which indicates that the eye is closed for the given BER under the input variation or jitter with 10% deviation. The verification time is in 110 seconds.

6. CONCLUSIONS

In this paper, a zonotoped reachability analysis is developed for the verification of high-speed I/O links considering both temporal and spatial variations. The zonotope is introduced to model both jitter and device parameter uncertainty to avoid multiple simulations within long input data sequence for the verification of the worst-case eye-diagram. Moreover, nonlinear zonotoped macro-model is further developed to reduce complexity by forming the zonotoped subspace or manifold. As shown by numerical experiments for high-speed I/O links considering temporal and spatial variations, zonotoped macromodel (order=7) based reachability analysis can generate the worst-case eye-diagram parameters with less than 6% error but with 450× speedup when compared to Monte Carlo simulations of the full model.

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