A Thermal Resilient Integration of Many-core Microprocessors and Main Memory by 2.5D TSI I/Os

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***Abstract*—One memory-logic-integration design platform is developed in this paper with thermal reliability analysis provided for 2.5D through-silicon-interposer (TSI) and 3D through-silicon-via (TSV) based integrations. Temperature-dependent delay and power models have been developed at microarchitecture level for 2.5D and 3D integrations of many-core microprocessors and main memory, respectively. Experiments are performed by general-purpose benchmarks from SPEC CPU2006 and also cloud-oriented benchmarks from Phoenix with the following observations. The memory-logic integration by 3D RC-interconnected TSV I/Os can result in thermal runaway failures due to strong electrical-thermal couplings. On the other hand, the one by 2.5D transmission-line-interconnected TSI I/Os has shown almost the same energy efficiency and better thermal resilience.**

I. Introduction

Many-core microprocessors with integrated main memory have become the recent interest for the design of high-performance servers. The 2D integration has low bandwidth, long latency and hence poor I/O energy efficiency, since limited data are transferred with long time. On the other hand, the 3D integration [1] by vertical stacking is one promising solution for memory-logic integration by through-silicon-via (TSV), which can significantly reduce the communication latency, improve communication bandwidth and hence result in high I/O energy efficiency.

However, the vertical stacking by TSV results in a long heat dissipation path, which significantly degrades the thermal reliability [2]. From device perspective, due to the isolation material (liner) that surrounds the TSV where the heat is accumulated, it can introduce significant delay [3]. From system perspective, memory-logic integration with high-density DRAMs has significant leakage current, which can be coupled with temperature to form a positive-feedback loop resulting in thermal runaway failure [4].

Instead of stacking memory and logic at different layers with TSV I/Os, the recent introduction of through-silicon-interposer (TSI) [5] provides a 2.5D solution for memory-logic integration. In contrast to TSV which is short RC-interconnect for inter-layer communication, TSI is usually designed as transmission line (T-line) targeted for high-speed long-distance communication between main memory and cores. Compared to the RC-interconnect with repeaters, 2D single-ended T-line (STL) or differential T-line (DTL) [6] with current-mode-logic (CML) buffers [7] have demonstrated better latency, power and bandwidth performance but with large area overhead. However the TSI based T-line can be designed through and under the common substrate, so high performance yet low area overhead memory-logic integration can be achieved. What is more, as memory and logic components are spread on the common substrate that is close to heat-sink, the thermal reliability of 2.5D integration by TSI I/Os can be better than 3D integration by TSV I/Os.

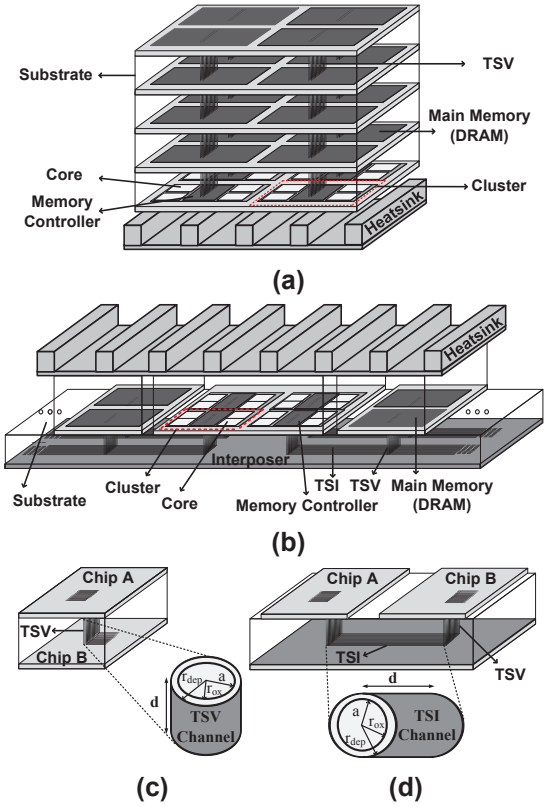

Fig. 1: (a) 3D integration by TSV I/O; (b) 2.5D integration by TSI I/O; (c) 3D TSV I/O structure; (d) 2.5D TSI I/O structure.

In this paper, we build up a memory-logic-integration design platform to evaluate thermal reliability of the integrated many-core microprocessors and main memory by 2.5D TSI-based I/Os and 3D TSV-based I/Os. With consideration of electrical-thermal coupling, detailed delay and power models of 2.5D and 3D I/Os are introduced into microarchitecture-level cycle-accurate simulators. With the use of general-purpose SPEC CPU2006 [8] and cloud-oriented Phoenix [9] benchmarks, the following results are observed. As for energy efficiency, the 2.5D integration shows almost the same efficiency as 3D integration when the temperature is high. Moreover, thermal runaway failure is prone to be observed in 3D integration by TSV I/Os with more than four layers.

978-3-9815370-2-4/DATE14/©2014 EDAA
Please address comments to haoyu@ntu.edu.sg. This work is sponsored by Singapore MOE TIER-2 fund MOE2010-T2-2-037 (ARC 5/11) and A*STAR SERC-PSF fund 11201202015.

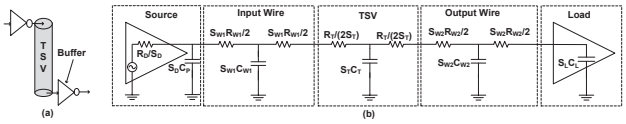

Fig. 2: Temperature-dependent delay model of one TSV RC-interconnect I/O channel.

II. 2.5D/3D Microarchitecture Platform

Figure 1 shows the platform of many-core microprocessors and main memory by 2.5D and 3D integrations. TSV and TSI are two I/O solutions considered in this memory-logic-integration design.

As shown in Figure 1(a), face-to-back bonding is applied between layers. As heat-sink is on the bottom, there is long heat dissipation path for 3D stacking. So the accumulated heat can affect the TSV I/Os performance severely. In contrast, for 2.5D bonding with TSI I/Os, four main memory banks and cores can be spread uniformly on substrate with close distance to heat-sink, as shown in Figure 1(b). As such, the thermal reliability concern would be relaxed in the 2.5D architecture. TSV I/Os in Figure 1(c) are used for vertical connection of chips on different levels of the same IC [10], which are usually designed as RC-interconnects. TSV I/Os can also be used for signal transmission and power propagation. While in Figure 1(d), TSI I/Os are utilized for horizontal connection of two chips on the same level but on the different ICs [5]. The substrate is drilled and TSIs are formed underneath to connect two dies. TSI I/Os for 2.5D bonding are usually designed as transmission lines. In the following, we will provide detailed physical models of 3D TSV and 2.5D TSI I/Os.

III. 2.5D/3D Delay and Bandwidth Model

The first thermal reliability concern of memory-logic by 2.5D or 3D integration is electrical-thermal coupling to delay.

A. Nonlinear Temperature Dependent Capacitor

The traditional 2D interconnect is modeled as RC-circuit with linear dependence to temperature. As shown in Figure 1(c), due to existence of liner material around TSV metal, depletion region is formed [5], [11] when signal voltage is applied across TSV. As such, TSV capacitance C_T and TSV resistance R_T can be modeled by

$$\frac{1}{C_T} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}; \quad R_T = \frac{\rho d}{\pi a^2} \tag{1}$$

- where C_{ox} and C_{dep} are liner and depletion region capacitance,
- ρ is resistivity of TSV material,
- d, a are the height of TSV and the outer radius of TSV metal.

Note that the presence of liner material around TSV forms a nonlinear capacitor against biasing voltage and temperature. The temperature dependent TSV model can be given as

$$R_T = R_0(1 + \alpha(T - T_0)); \quad C_T = C_0 + \beta_1 T + \beta_2 T^2 \tag{2}$$

- where R_0 and C_0 are resistance and capacitance of TSV or TSI at room temperature T_0,
- α is the temperature dependent coefficient for resistance,
- β_1, β_2 are temperature dependent first and second order coefficients of capacitance.

All the coefficients can be characterized from measurement [11].

B. Temperature-dependent Delay Model of TSV

A TSV-based 3D I/O channel with buffers at both ends is shown in Figure 2(a). We use the inverter as the buffer for TSV. The corresponding delay model for one TSV I/O channel with capacitance C_T modeled by (2) is shown in Figure 2(b). Based on the TSV resistance R_T and capacitance C_T in (1), the delay of one TSV I/O channel is given by

$$D_{3d-io} = R_{in}\alpha\beta_2 T^3 + R_{in}[(1-\alpha T_0)\beta_2 + \alpha\beta_1]T^2 + [\alpha(D_0 + R_{in}C_0) + (1-\alpha T_0)R_{in}\beta_1]T + (1-\alpha T_0)(R_{in}C_0 + D_0) \tag{3}$$

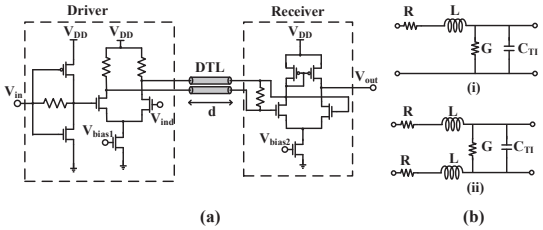

Fig. 3: Temperature-dependent delay model of TSI I/O channel.

- where R_{in} is the total resistance seen from TSV capacitor C_T,
- D_0 is the delay of the circuit without TSV.

As such, for one TSV I/O channel with delay D_{3d-io} given in (3), the corresponding bandwidth BW_{TSV} for N TSV channels can be given as $BW_{TSV} = \frac{N}{D_{3d-io}}$. In addition, from (3), it can be observed that the delay of TSV based I/O channel can vary nonlinearly with the temperature, which may cause significant thermal reliability concern.

C. Temperature-dependent Delay Model of TSI

Because the heat-sink in 2.5D is much closer to the substrate layer than that in 3D, there would be less hotspots and temperature gradient in 2.5D. As shown in Figure 1(d), one can fabricate TSI underneath the substrate to connect two chips with no TSI area overhead. As such, it is possible to realize T-line by TSI for high-speed and low-power 2.5D I/Os as shown in Figure 3(a). Note that delay of T-line depends on the characteristic impedance and takeover frequency under single-ended and differential modes [12]. The current-mode-logic (CML) buffer [7] is used as driver for T-line, which is a differential digital logic that can transmit data at high frequency.

A single-ended T-line (STL) is shown in Figure 3(b)(i). For a differential T-line (DTL) in Figure 3(b)(ii), there exists mutual inductive and capacitive coupling. The characteristic impedance of STL and DTL are

$$Z_{STL} = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C_{TI})}}; \quad Z_{DTL} = 2\sqrt{\frac{(L - L_m)}{(C_{TI} + C_m)}} \tag{4}$$

where C_{TI} is the temperature dependent TSI capacitance from (2), R, L, G are resistance, inductance and shunt conductance per unit length, and C_m, L_m are mutual inductance and capacitance of DTL.

When a T-line is designed to operate above takeover frequency, it will work in LC region with delay of

$$D_{TSI} = \frac{1}{\omega}\sqrt{Im(\gamma Z_0) \times Im(\frac{\gamma}{Z_0})} \tag{5}$$

- where $Im(x)$ is imaginary part and γ is propagation constant,
- the characteristic impedance from (4) becomes $Z_0 = \sqrt{\frac{L}{C_{TI}}}$ for STL and $Z_0 = 2\sqrt{\frac{L}{C_{TI}}}$ for DTL.

Thus, the delay can be written as a function of inductance L and capacitance C_{TI}, which is nonlinearly dependent on temperature T. The delay of 2.5D I/O based on (5) can be given as

$$D_{2.5d-io} = R_D C_L + 2\sqrt{LC_{TI}} \tag{6}$$

- where R_D and C_L are driver impedance and load capacitance.

When compared to the temperature-dependent delay model of 3D TSV in (3), one can observe that the temperature dependence of 2.5D TSI given in (6) is much weaker with square-root dependence. This makes 2.5D TSI delay less prone to temperature variation. What is more, the temperature gradient is also much smaller. Similarly, the bandwidth for TSI with N channels can be given by $BW_{TSI} = \frac{N}{D_{2.5d-io}}$. As the delay of 2.5D TSI has much smaller dependence with temperature than 3D TSV, the impact of temperature on bandwidth and delay is small, which means that a more thermal resilient design can be achieved in 2.5D integration.

IV. 2.5D/3D Power and Thermal Model

A. Power Models

As shown in Figure 1, the 2.5D and 3D integrations consist of cores, memory and I/O channel. The power model of each component needs to be studied for thermal analysis.

1) Core and DRAM Power Model: Core power P_{core_total} is the sum of dynamic power P_{core_dyn} and leakage power P_{core_leak},

$$P_{core\_total} = \underbrace{\eta * C_{core} * V_{DD} * \Delta V * f}_{P_{core\_dyn}} + \underbrace{V_{DD} * I_{leakage}}_{P_{core\_leak}} \quad (7)$$

with

$$I_{leakage} = A_s \cdot \frac{W_d}{L_d} \cdot v_T^2 (1 - e^{\frac{-V_{DS}}{v_T}}) \cdot e^{\frac{V_{GS} - V_{th}}{ns \cdot v_T}} \quad (8)$$

- where V_{DD} is the supply voltage with ΔV swing,
- C_{core} is the core load capacitance,
- η represents the activity factor and f is the clock frequency,
- L_d and W_d are the effective device channel length and width,
- A_s is technology-dependent constants, ns is the subthreshold swing coefficient and $v_T = \frac{k \cdot T}{q}$ is the thermal voltage.

The dynamic DRAM power with a data array of n identical banks and each bank has B I/O channels can be given as

$$P_{DRAM\_dyn} = n * B * \eta * C_{channel} * V_{DD}^2 * f \quad (9)$$

- where $C_{channel}$ is the channel capacitance.

Assuming that one DRAM memory bank with size of M has leakage current similar to (8), the leakage DRAM power can be given as

$$P_{DRAM\_leak} = n * M * V_{DD} * I_{leakage} \quad (10)$$

It can be observed that the leakage current can vary significantly with temperature in an exponential fashion which may lead to two consequences. Firstly, the leakage power can dominate the total power. Secondly, it may form a positive feedback loop with temperature that can lead to thermal runaway failure.

2) I/O Power Model: The dynamic power of 3D I/O with N-channel TSVs and buffers can be given as

$$P_{3d-io} = \eta * N * (C_T + C_L) * V_{DD}^2 * f \quad (11)$$

- where η represents the activity factor,
- C_T is the temperature dependent capacitance given in (2),
- C_L is the load capacitance of the buffer.

Based on (11), for a TSV I/O channel operating at a high temperature, the dynamic power will go up significantly due to the nonlinear temperature dependence of capacitance. The dynamic power of 2.5D I/O with N-channel TSIs and buffers can be calculated as [13]

$$P_{2.5d-io} = \frac{\eta * N * V_{DD}^2 * s}{(R_D + Z_0)} * f \quad (12)$$

- where s is the duration of signal pulse, η is the activity factor,
- Z_0 is the characteristic impedance from (5),
- R_D is the driver impedance of CML buffer.

By observing (5) and (12), it can be concluded that the power of TSI I/O channel is less dependent on temperature (with square-root dependence) than TSV I/O channel (with quadratic dependence).

B. Thermal Runaway Failure

The second thermal reliability concern is between power and temperature. Under large bandwidth, it is more liable to form a positive feedback loop resulting in thermal runaway failure. The thermal dynamics with heat-sink heat removal ability is [14]

$$C_{TR} \frac{dT}{dt} = P_{thermal} - \sum_{j=1}^{g} \frac{T - T_j}{R_j} \quad (13)$$

- where $P_{thermal}$ is thermal power, C_{TR} is thermal capacitance,
- R_j is the thermal resistance path from g chips to the heat-sink.

If the thermal source grows much faster than heat removal ability of heat-sink, temperature will increase exponentially. Thermal runaway temperature $T_{threshold}$ is temperature at which thermal runaway failure happens. To avoid thermal runaway failure, we can place heat-sink closer to processing cores. Since 2.5D integration has a much close heat-removal path to heat-sink, it shows better heat removal ability than 3D integration.

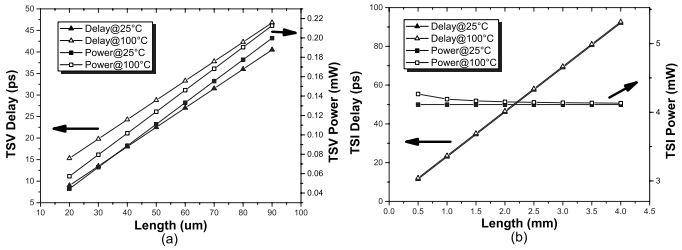

Fig. 4: Delay and power comparison under different length for (a) TSV I/Os; (b) TSI I/Os.

V. Experimental Results

A. Experiment Setup

The system setup for microarchitecture evaluation platform is shown in in Table I. The simulation is performed in gem5 [15] with multi-core system set up as 16-core x86 microprocessors. Benchmarks from SPEC CPU2006 [8] and Phoenix [9] are used. The performance results from gem5 are then sent to McPAT [16] to analyze cores scaled at 22nm. CACTI [17] is used to model DRAMs scaled at 32nm. The area estimations are obtained from simulation results.

In addition, the number of I/O channels for both 2.5D and 3D integrations is 64. The length of TSV I/Os is $50um$, which is the distance of adjacent layers. The length of TSI I/Os is $1.5mm$, which is the distance between two ICs. Then the total area is about $288mm^2$ for 2.5D integration and $64mm^2$ for 3D integration. Moreover, a thermal simulator [18] is employed to provide temperature profiles for thermal runaway failure observations in both integrations.

TABLE I: System setup for microarchitecture evaluation platform

Components	Description	Value	Area Estimation
Core	Frequency	1.0 GHz	2.469 mm^2
	L1 cache size	32 KByte	
	Cacheline size	64 Byte	
DRAM	Number of banks	4	32.025 mm^2
	Bank size	64 MByte	
TSV I/Os	Number of channels	64	19 μm^2
	Length of interconnect	50 um	
TSI I/Os	Number of channels	64	10 μm^2
	Length of interconnect	1.5 mm	

B. Device and System Model Results

1) Device Model Results: We first study the delay and power realations with interconnect length in Figure 4. At $25°C$, the delay of TSV is around $22.50ps$ in $50\mu m$ and $40.50ps$ in $90\mu m$ with linear relation as well as power with $0.11mW$ in $50\mu m$ and $0.20mW$ in $90\mu m$. While at $25°C$, the delay of TSI is around $34.52ps$ in $1.5mm$ and $69.04ps$ in $3.0mm$ length, also with linear relation. The power of TSI is $4.11mW$ in all length. Compared to the TSV I/Os, the power of TSI I/Os shows little dependence on the interconnect length.

Next, the delay and power relations with temperature is shown in Figure 5. The nonlinear temperature-dependent capacitance has more effect on TSV I/Os. For example, the delays of TSV and TSI are $22.50ps$ and $34.52ps$ at $25°C$. When the temperature rises to $130°C$, the delays become $31.95ps$ and $35.53ps$, with increase of 42% and 3%, respectively. As such, TSV I/Os delay is more sensitive to the temperature. With the same temperature transition, the power of TSV and TSI show increase change by 20% and 2%.

2) System Model Results: We further study the system level performance of two integrations with system power breakdown shown in Figure 6. DRAM power is the dominant factor in the system. For example in Figure 6(b), the DRAM power accounts for 65.33% with the core power accounts for just 34.24%. The TSI I/Os power is less than 6% of whole system power consumption and it is insensitive to the temperature. While the TSV I/Os power contributes less than 4% of the whole system power consumption. With the temperature rising, TSV I/Os power percentage will also increase.

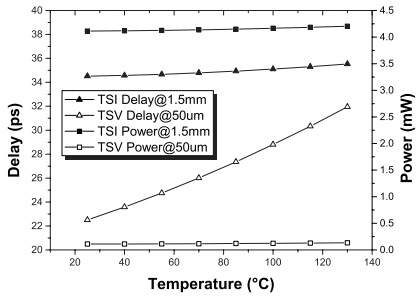

Fig. 5: Delay and power comparison under different temperature for TSV I/Os and TSI I/Os.

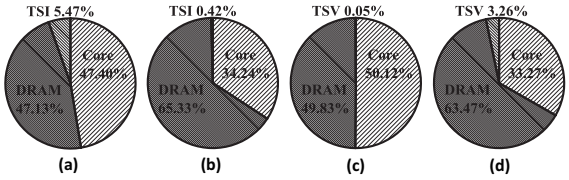

Fig. 6: Power breakdown of (a) 2.5D integration at $25°C$; (b) 2.5D integration at $120°C$; (c) 3D integration at $25°C$; (d) 3D integration at $120°C$.

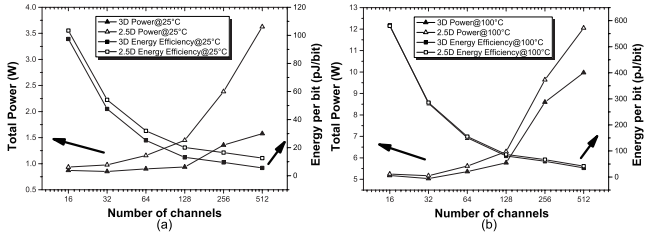

Fig. 7: Total power and energy efficiency with different bandwidths: (a) at $25°C$; (b) at $100°C$.

We now present the power and energy efficiency relation with bandwidth in Figure 7. The bandwidth can be adjusted by varying the number of I/O channels. On average, 2.5D integration consumes 62% more power than 3D integration at $25°C$. When the temperature rises to $100°C$, it consumes 10% more power. If heat dissipation is not well designed, it will form a positive feedback loop between leakage power and temperature resulting thermal runaway failure. Note that the delay of the TSVs will be greatly affected when the temperature is high, thus decrease the bandwidth. Here the energy efficiency is defined as energy consumption per bit. It can be seen that energy efficiency will decrease as the number of channel increases. On average, 2.5D integration consumes 21% more energy per bit than 3D integration at $25°C$. But when the temperature rises to $100°C$, 2.5D integration achieves almost the same energy efficiency as 3D integration.

In the following, we will explore the thermal runaway issue in both integrations. The initial temperature is set at $25°C$. The heat-sink size is $4.0cm \times 4.0cm$ for 2.5D integration and $2.0cm \times 2.0cm$ for 3D integration, both with heat-removal resistance of $4.6K/W$. The system temperature trend is shown in Figure 8. When the temperature goes beyond the threshold temperature $(100°C)$, thermal runaway failure happens. The temperature of 2.5D integration is maintained between $50°C$ and $70°C$. For 3D integration, we vary the the number of memory layers to see its heat dissipation performance. We can see that it remains stable below 4 layers. With 5 layers, the temperature rising trends can be observed after 6 millions execution cycles, which rises quickly beyond $100°C$. Note that the number of memory layers will affect the system performance. As such, high performance 3D system is more liable to the risk of thermal runaway issue. In this case, 4 layers setting is the best from thermal perspective.

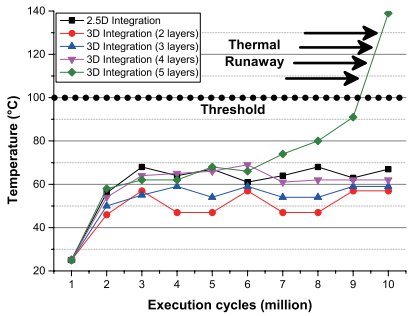

Fig. 8: Thermal runaway analysis by 3D and 2.5D integrations.

VI. Conclusions

Thermal resilient memory-logic-integration is studied in this paper by 2.5D TSI I/Os with comparison to 3D TSV I/Os. Detailed electrical-thermal coupled delay and thermal models are developed. The 3D TSV RC-interconnect based I/Os show better delay and bandwidth performance but are more sensitive to the temperature when considering poor thermal-conductive isolation layer and leakage-intensive memory. The 2.5D TSI T-line based I/Os have much less electrical-thermal coupling to delay and power, hence are more resilient to temperature-dependent thermal runaway failure. Moreover, the low-area-overhead 2.5D TSI based integration can achieve similar bandwidth and power performance as 3D TSV based integration.

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