High-Speed and Low-Power 2.5D I/O Circuits for Memory-logic-integration by Through-Silicon Interposer

Jiacheng Wang[*‡], Shunli Ma[†‡], Sai Manoj P. D.[‡], Mingbin Yu[§], Roshan Weerasekera[§], Hao Yu[‡]

[*]ERI@N, Interdisciplinary Graduate School, Nanyang Technological University, Singapore
[†]State Key Lab of ASIC and System, Fudan Univerisy, China
[‡]School of EEE, Nanyang Technological Univerisy, Singapore 639798
[§]Institute of Microelectronics, A*STAR, Singapore
Email: haoyu@ntu.edu.sg

Abstract—In this paper, two high-speed and low-power I/O circuits are developed using through-silicon-interposer (TSI) for 2.5D integration of multi-core processor and memory in 65nm CMOS process. For a 3mm TSI interconnection of transmission line (T-line), the first I/O circuit is a low-voltage-differential-signal (LVDS) buffer and the second one is a current-mode-logic (CML) buffer. To compensate the high-frequency loss from T-line, a pre-emphasis circuit is deployed in the LVDS buffer, and a wide-band inductor-matching is deployed in the CML buffer. Based on the post layout simulation results, the LVDS buffer can achieve 360mV peak-to-peak differential output signal swing and 563fs cycle-to-cycle jitter with 10Gb/s bandwidth and 4.8mW power consumption. The CML buffer can achieve 240mV peak-to-peak differential output signal swing and 453fs jitter with 12.8Gb/s data-rate and 1.6mA current consumption under 0.6V ultra low-power supply.

I. INTRODUCTION

Due to rapid growth in application data, there is emerging design for energy efficient cloud-server to handle big-data applications. Such a energy-efficient cloud-server design requires integration of multi-core microprocessors with high density main memory on a single chip [1]. The three-dimensional (3D) stacking for memory-logic-integration by through-silicon-via (TSV) is one promising solution, but it has limited thermal and mechanical reliabilities when stacking multiple layers [2]–[4]. The through-silicon-interposer (TSI), or the so called 2.5D integration, has become an alternative solution for memory-logic-integration with significantly improved thermal and mechanical reliabilities compared to the 3D TSVs [5]. The sketch diagram of TSV and TSI interconnections are shown in Fig. 1. One can observe that transmission line (T-line) can be implemented in a 2.5D fashion with TSI trace under the common substrate, which consumes less area yet with reduced latency and improved bandwidth.

However, different from the RC-interconnect based I/O scheme by 3D TSV, the challenge of 2.5D TSI is to design a high-speed and low-power I/O i.e., a serial data link with high data-rate per Joule. The recent microprocessor I/O in [6] has achieved high-speed performance with less than $1pJ/bit$ in 2D integration. But there are no works to address the 2.5D I/O
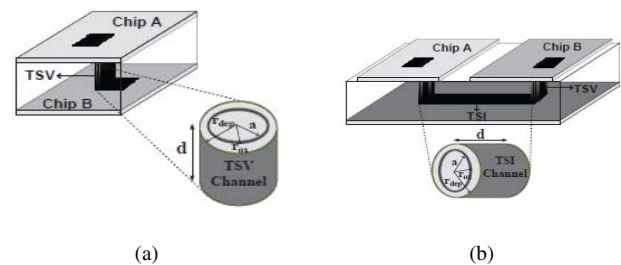

Fig. 1. (a) Interconnection between two chips by TSV, (b) Interconnection between two chips by TSI

designs for TSI based T-line. In this paper, two high-speed and low-power I/O circuits are developed for 2.5D TSI T-line with 3mm-length in 65nm CMOS process: one is a low-voltage-differential-signal (LVDS) buffer; and the other is a current-mode-logic (CML) buffer. In order to overcome the loss of TSI T-line at high frequency, a pre-emphasis technique is proposed in the LVDS buffer; and a wide-band matching by inductor is deployed in the CML buffer. Based on the post layout simulation results, the LVDS and CML buffers are capable of $10Gb/s$ and $12.8Gb/s$ operational data rate, while achieving an energy efficiency of $0.48pJ/bit$ and $0.075pJ/bit$, respectively.

The rest of this paper is organized as follows: Section II presents the I/O circuit architecture for 2.5D TSI T-line. Section III describes the details of the developed two high-speed low-power I/O circuits. In Section IV, layouts of the two I/O circuits are illustrated with supported simulation results in 65nm CMOS process. Finally, Section V concludes the paper.

II. 2.5D I/O FOR TSI T-LINE

The memory-logic-integration in this work assumes that all multi-core processors have shared memory [7], [8]. The cores and memories can be fabricated by different manufacturing processes, and then integrated on one common substrate by silicon interposer underneath. The 2.5D integration can significantly improve the bandwidth and reduce the power
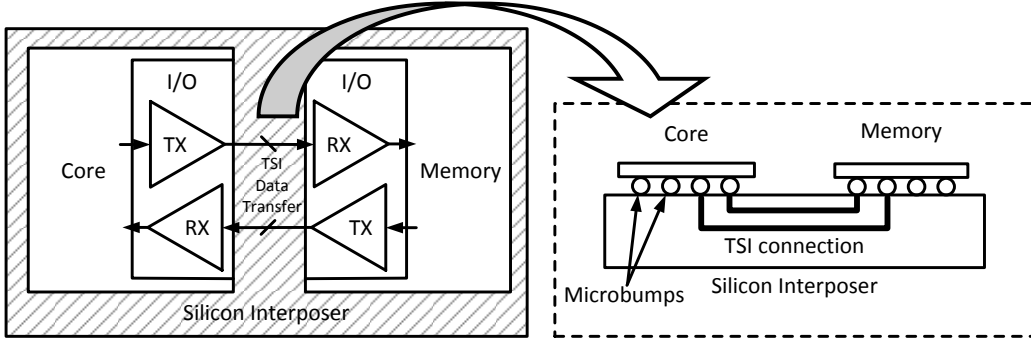
Fig. 2. 2.5D TSI I/O interconnection between core and memories its cross section view

consumption when compared to the conventional multi-chip modules (MCM), in which wire-bonding and PCB-level T-line have introduced significant latency and power efficiency [9].

The architecture of the high-speed low-power I/O for 2.5D TSI is illustrated in Fig. 2. One can observe that signals from digital logic of core are transferred to I/O circuits, and then transmitted or received as differential signals at the two chips. All I/Os in the core and memory are attached to microbumps, which are used to make TSI connection in silicon substrate.

At high frequencies, there is frequency-loss from TSI T-line. For example, the resistance of the T-line increases with frequency as,

$$G_{skin}(f) = e^{-(1+j)l\sqrt{\pi\mu\sigma f}} \tag{1}$$

where l is the T-line length, μ is the permeability, and σ is the conductivity.

Similarly, the dielectric loss is

$$G_{di}(f) = e^{-l\sqrt{\varepsilon_r}tan\delta f/c} \tag{2}$$

where ε_r is the dielectric constant, $tan\delta$ is the loss tangent of material, and c is the speed of light [10]. As such, one needs to develop methods to compensate the frequency-dependent loss for 2.5D TSI T-line based I/O designs.
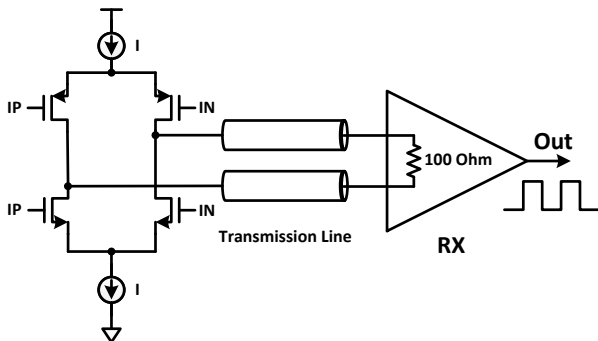

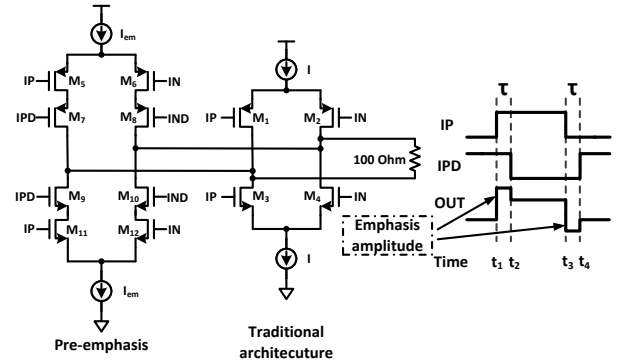Fig. 3. Typical LVDS I/O architecture

Fig. 4. A LVDS transmitter with pre-emphasis technique

III. DESIGN OF 2.5D I/Os

A. LVDS I/O Buffer

Typical LVDS interface shown in Fig. 3 consists of a current source with nominal $3.5mA$, which drives the differential TSI T-lines terminated with 100Ω load. The LVDS receivers have high input impedance and the driving current mainly flows through the 100Ω termination resistor, thereby creating a valid logic "one" or "zero" [11]. The resistor at the receiver end can not only provide the optimum T-line impedance matching, but also acts as the load resistor of current source to generate a low-voltage swing of $250mV - 400mV$.

Considering the loss of TSI T-line discussed in section II, to improve margins of the data eye-diagram, an amplitude pre-emphasis is used in the LVDS design. The schematic of LVDS transmitter is shown in Fig 4. In the left part, transistors M_5-M_{12} contribute to a pre-emphasized signal generation. The signal IP and IN are differential data signals coming from digital logic input, and IPD and IND are the reverse input data delayed by a time constant τ.

Assume that the amplitude of pre-emphasis gain is G, i.e., the ratio of current in the pre-emphasis driver and the normal driver, I_{em}/I. The transfer function for the pre-emphasized stage can be expressed as,

$$H_{pre-em} = \frac{\tau A(s)}{A(s)} = I \cdot (1 - Ge^{-s\tau}) \tag{3}$$

where $A(s)$ is the transfer function of normal LVDS transmitter. When a first-order Pade approximation is used in this function, one can have

$$H_{pre-em} = I \cdot (1 - G\frac{1 - s(\tau/2)}{1 + s(\tau/2)})$$
$$= I \cdot (1 - G)\frac{1 + s(\tau/2)(1 + G)/(1 - G)}{1 + s(\tau/2)} \quad (4)$$

Equation (4) reveals that the amplitude pre-emphasis can reduce the DC gain, but can enhance the high frequency response. The transfer function has an additional pole at $1/\tau$. The high frequency compensation, which is $\pm(1 + G)$ in equation (4), is performed when there is a data transition. In this design, we use the digital inverter chain to delay the input digital signals with time constant $\tau = 45ps$. In order to achieve the low-power consumption, the current source of LVDS buffer is controlled to drive about only $350mV$ peak-to-peak voltage swing at the termination resistor. And the ratio of pre-emphasis current gain is $G = 0.28$.

The operation of the overall LVDS buffer is explained with the time chart in Fig. 4 as follows. When IP is high at the time instant t_1, switches $M_{2,3,6,11}$ are turned on. The main current I flows into a termination resistor to generate the output voltage. At the same time, the delayed and reverse signal IPD is high to turn on transistors M_8 and M_9 at the time instant t_2. So, during the period between t_1 and t_2, the amplitude of the output is driven by the sum of two current sources, I and I_{em}. As such, one can achieve a higher voltage swing at the output rising-edge that can compensate the high frequency loss. Similarly, in the period between t_3 and t_4, the output falling-edge is emphasized.

B. CML I/O Buffer

We have also explored the design of current-mode-logic (CML) buffer for 2.5D TSI T-line. CML is a differential digital logic that can transmit data at high frequency.

As shown in Fig 5, a two-stage CML transmitter is designed with a pre-amp stage. A chain of two CML buffers is used such that the output of pre-amp stage is connected to the input of driving stage. When the digital logic input is in, the differential branches of CML buffers are ON and OFF that are controlled by two input transistors M_1 and M_2. Note that the CML buffer requires a full current switching and the current flows through the ON branch only. In this design, there is no tail current used to achieve a full current swing. The currents through the resistor and inductor loads are just controlled by the input voltage swing of two transistors (V_{GS}) and their size. Thus the size of two pair of transistors are designed carefully in order to provide enough driving ability with low current consumption at the same time.

Moreover, we need the CML buffer to drive load through the microbump pad with 3mm TSI T-line, which has smaller load than the bonding wire with package trace. This means that NMOS transistors of the second stage CML buffer in Fig. 5 can have smaller size and smaller gate-to-channel capacitance.
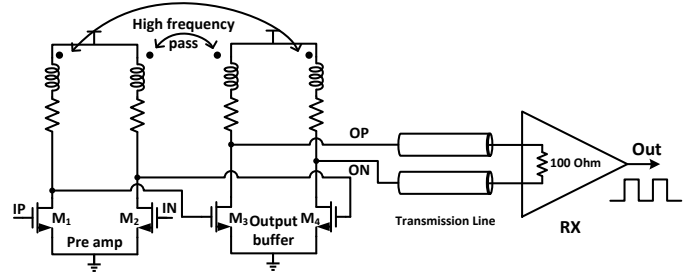

Fig. 5. A schematic of the proposed CML I/O interface

Thus, we can use as low as $0.6V$ power supply to decrease the power consumption.

Furthermore, to compensate high frequency loss of a 2.5D TSI T-line, inductor loads are designed as cross coupled. As such, there is a fast data-pass through inductors when the CML buffer transmits high speed signal. The first-stage of CML transmitter works as a pre-amplifier, which can provide a common mode voltage input to the next stage to guarantee the two input pairs of NMOS in the second stage working in saturation region all the time.

IV. POST LAYOUT SIMULATION RESULTS

For the 2.5D TSI based integration in this paper, all chips are assembled face down and are attached to microbumps. They are connected through around $20\mu m$ width TSI T-line through one common substrate. The I/O circuits are the communication units to deliver data signals between cores and memories. The TSI T-line is by aluminum, and the dielectric is silicon dioxide. This T-line length, width and characteristic impedance are $3mm$, $20\mu m$ and 50Ω, respectively.

The simulation results of TSI T-line model are shown in Fig. 6. From simulation results, at $5GHz$ signal frequency which means that the data-rate is at $10GHz$, one can observe that the delay of T-line is $38°$ (10ps in the time domain); and the loss is roughly $0.9dB$.

The two I/O Interface circuits are designed in UMC 65nm CMOS process using 1P6M layers. Fig 7 illustrates the layout of LVDS and CML transceiver circuits. In the figure, there are six microbumps distributed in the surrounding (the yellow octagons), which are used for microbumps fabricated and TSI connection between chips. The whole chip area is $550\mu m \times 330\mu m$, with about $60\mu m \times 120\mu m$ area for LVDS transceiver. In CML circuits, the inductors cost most area of the chip, which are $90\mu m \times 90\mu m$ for each.

Fig. 8 and Fig. 9 show the post layout simulation results of the two I/O circuits. From Fig. 8, it can be observed that the LVDS I/O interface can achieve $360mV$ peak-to-peak output swing and $563fs$ cycle-to-cycle jitter with $10GHz$ bandwidth. This waveform consists about $2dB$ amplitude pre-emphasis with the 0.28 ratio of current between emphasis and mean circuit. And the power consumption is only $4.8mW$ under $1.2V$ supply, which is about $0.48pJ/b$ energy efficiency. And in Fig. 8(b), when the signals are transmitted through the TSI transmission lines between chips, the signal has $30mV$ loss in
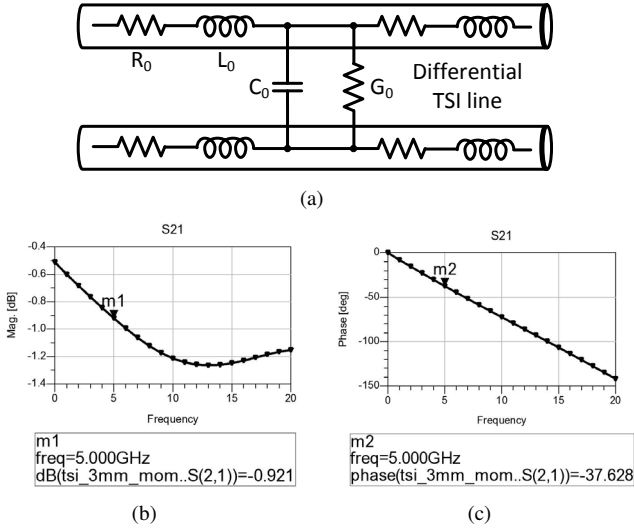
(a)

(b)

(c)

Fig. 6. (a) General characteristics of TSI transmission line, (b) Loss of a 3mm TSI in different frequency, (c) Delay of a 3mm TSI line

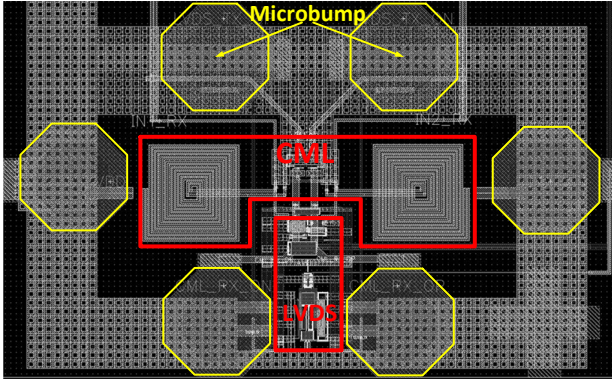Fig. 7. Layout of two I/O Interface

(a)

(b)

Fig. 8. (a) Simulation waveform of LVDS output eyediagram, (b) Waveform of LVDS passed through TSI connection

(a)

(b)

Fig. 9. (a) Simulation waveform of CML output eyediagram, (b) Waveform of CML passed through TSI connection

simulation. But the $2dB$ amplitude pre-emphasis part, which compensate the loss exactly, can protect the performance of high frequency edges. For the CML circuits, it can work under only $0.6V$ power supply, with $1.6mA$ total current consumption due to amplitude boosted inductors. As shown in Fig. 9, it can provide $240mV$ peak-to-peak differential signal swing and $453fs$ jitter with $12.8Gb/s$ bandwidth, and $196mV$ peak-to-peak voltage after TSI T-line loss.

V. CONCLUSION

In this paper, we investigated the 2.5 I/O circuit designs based on TSI T-line. There are two high-speed low-power I/O circuits developed: one is LVDS buffer and the other is CML buffer, both for a $3mm$ TSI T-line towards multi-core and memory integration. To compensate the loss of TSI T-line in high frequency, pre-emphasis is used in the LVDS buffer and wide-band inductor matching is used in the CML buffer. Both I/O buffers are designed in UMC 65nm CMOS process. Post layout simulation results show that the proposed LVDS buffer and CML buffer are capable of providing speed at $10Gb/s$ and $12.8Gb/s$ with $0.48pJ/bit$ and $0.075pJ/bit$ efficiency.
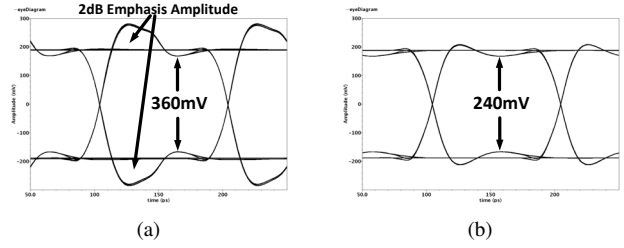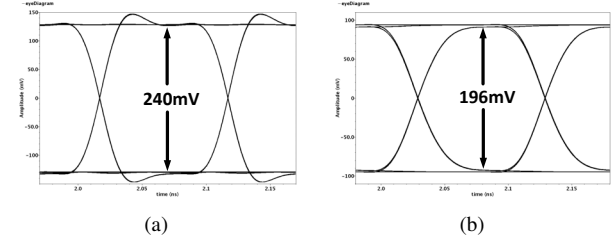
REFERENCES

[1] U. Kang *et al.*, "8 Gb 3-D DDR3 DRAM Using Through-Silicon-Via Technology," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 1, pp. 111–119, 2010.

[2] H. Qian *et al.*, "Real-Time Thermal Management of 3D Multi-Core System with Fine-Grained Cooling Control," in *IEEE International 3D Systems Integration Conference (3DIC)*, 2010.

[3] X. Huang, H. Yu, and W. Zhang, "NEMS Based Thermal Management for 3D Many-Core System," in *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, 2011.

[4] Y. Shang *et al.*, "Thermal-Reliable 3D Clock-Tree Synthesis Considering Nonlinear Electrical-Thermal-Coupled TSV Model," in *Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2013.

[5] H. Yu, J. Ho, and L. He, "Allocating Power Ground Vias in 3D ICs for Simultaneous Power and Thermal Integrity," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 14, no. 3, p. 41, 2009.

[6] F. O'Mahony *et al.*, "The future of electrical I/O for microprocessors," in *International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, 2009.

[7] Z. Yu *et al.*, "An 800MHz 320mW 16-Core Processor with Message-Passing and Shared-Memory Inter-Core Communication Mechanisms," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2012.

[8] J. Howard *et al.*, "A 48-Core IA-32 Message-Passing Processor with DVFS in 45nm CMOS," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2010.

[9] J. A. Plaza *et al.*, "Piezoresistive Accelerometers for MCM Package," *Journal of Microelectromechanical Systems*, vol. 11, no. 6, pp. 794–801, 2002.

[10] A. Deutsch, "Electrical Characteristics of Interconnections for High-Performance Systems," *Proceedings of the IEEE*, vol. 86, no. 2, pp. 315–357, 1998.

[11] M. Chen *et al.*, "Low-Voltage Low-Power LVDS Drivers," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 2, pp. 472–479, 2005.