Curriculum Vitae - Sai Manoj Pudukotai Dinakarrao

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Professional Experience

Assistant Professor Aug 2019-
Research Assistant Professor Sep 2018- Aug 2019
Post-Doctoral Research Fellow Nov 2017- Sep 2018
George Mason University, Dept. of Electrical and Computer Engineering
Research Topics: Adversarial learning, neuromorphic computing, machine learning (ML) for embedded systems' security, hardware accelerator design, security against reverse engineering of ICs, graph convolutional networks, security in IoT devices and networks, big-data analytics

Post-doctoral Researcher Mar 2015- Nov 2017
Vienna University of Technology (TU Wien), Inst. of Computer Technology
Research Topics: Neuromorphic computing, hardware accelerator design, self-aware many-core systems, Memristors for neuromorphic computing, FPGA design for industrial systems
Mentor: Prof. Axel Jantsch

Visiting Researcher Jan 2012- June 2012
Technical University of Kaiserslautern, Dept. of Electrical and Computer Engineering
Research Topics: LDPC decoder design for high-speed error-free wireless communication
Mentor: Prof. Norbert Wehn

Teaching Assistant Aug 2011- Dec 2011
International Institute of Information Technology Bangalore (IIITB), India
Topics: Wireless Sensor Networks
Mentor: Prof. Jyotsna Bapat

Education

Doctor of Philosophy (Ph. D.) Aug 2012- Nov 2015
Nanyang Technological University, Dept. of Electrical and Electronic Engineering, Singapore
Thesis title: 2.5D and 3D I/O Designs for Energy-efficient Memory-logic Integration towards Thousand-core On-chip
CGPA: 4.00/5.00
Advisor: Prof. Hao Yu

Master of Technology (M. Tech) July 2010- June 2012
International Institute of Information Technology Bangalore (IIITB), India
Thesis title: Design of LDPC Decoder with Optimal and Sub-optimal Decoding Schemes
CGPA: 3.57/4.00

Bachelor of Technology (B. Tech) Aug 2006- June 2010
Jawaharlal Nehru Technological University (JNTU) Anantapur, India
Thesis title: Multi-Micro-core Network-on-Chip on Spartan-3E FPGA
CGPA: 7.50/10.00

Research Interests

- Machine Learning and it's Security
  - Adversarial learning and vulnerabilities in machine learning
  - Defenses against adversarial attacks
- Hardware Security and Trust
  - Signature analysis of side-channel and malware attacks on CMPs
  - Adversarial attack to secure hardware against side-channel attacks
  - Adversarial attack to create undetectable side-channel attacks and malware
  - Adversarial attack to secure hardware against invasive reverse engineering
  - Detection and confinement of malware in IoT networks
- Hardware Architecture Design and Management
  - Design space exploration of FPGA+CPU architectures for high-performance data processing
  - Energy-efficient accelerator design for real-time image processing
  - FPGA+CPU based time-series processing of industrial data
  - Neuromorphic computing for on-chip fitting of large-sized deep neural networks
- Big-Data Analytics
  - Big-data computing algorithms for energy-efficient computing and acceleration
  - Emerging big-data application benchmarking and characterization on heterogeneous architecture
  - Application-architecture mapping and co-scheduling of big-data applications in servers
- Many-core Reliability and Resource Management
  - Reliability-aware many-core system design
  - Resource-aware many-core system design
  - On-chip communication and computation power optimization with cognitive methods

Awards and Recognitions

- "A Fast and Resource Efficient FPGA Implementation of Secret Sharing for Storage Applications" **nominated for Best paper award in ACM/IEEE Design Automation and Test in Europe (DATE) Conference, 2018**
- "Hardware acceleration of cryptographic procedures for secure distributed storage systems" by Jakob Stangl **won the TU Wien best Master thesis Dissertations award** (Role: Supervisor)
- **Winner of Xilinx Open Hardware Contest 2017** (Student category; Role: Supervisor) Xilinx Open Hardware 2017 Results
- Participant of Europe Innovate Contest 2017
- **Student paper competition finalist** in IEEE International Microwave Symposium (IMS), 2015.
- **Recipient of 'A. Richard Newton Young Research Fellow Award'** in Design Automation Conference, 2013.

Equipment Support from Industry

- Xilinx corporation, 2 Xilinx Zedboards, 6 Vivado licenses for FPFA based cryptographic accelerators for servers (price: 830 €) - year: 2016

Invited Talks and Organized Workshops

11/2018 Special Session Organizer on "Is Adversarial Learning a Threat for Machine Learning? Defense Strategies and Design of Better Machine Learners!" at IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Diego, USA

09/2018 Special Session Organizer on "Towards Secure Computer Architecture: Understanding Security Vulnerabilities and Emerging Attacks for Better Defenses" at Embedded Systems Week (ESWEEK), Torino, Italy.

06/2017 Special Session Organizer on "Beyond Deep learning" at Design Automation Conference (DAC), Austin, USA

09/2016 Workshop "Cyber-Physical Systems" at Heidelberg Laureate Forum, Germany

08/2016 Invited talk "Resource Management and Self-learning in Micro-scale Systems" at Indian Institute of Technology (IIT) Madras, India

Supervising Ph.D. Students

Rakibul Hassan (George Mason University, Fairfax, USA)
Thesis Title: *Deep Learning for Security in IoT Networks*
Status: In progress (Started in August 2018)

Abhijitt Dhavlle (George Mason University, Fairfax, USA)
Thesis Title: *Side-Channel Attack Generation, Detection and Prevention*
Status: In progress (Started in January 2019)

Sanket Shukla (George Mason University, Fairfax, USA)
Thesis Title: *Ontology-based Malware Detection*
Status: In progress (Started in January 2019)

Wess Matthias (TU Wien and Siemens, Vienna, Austria)
Thesis Title: *Deep Learning on FPGAs for Industrial Big-Data Processing*
Status: In progress (Started in March 2017)

Martin Lechner (TU Wien and Mission Embedded, Vienna, Austria)
Thesis Title: *Accelerator Design and Automated Architectural Design for High-performance DNNs*
Status: In progress (Started in March 2018)

Supervised Master Students

Martin Lechner (M.Sc 2018, TU Wien)
Thesis Title: *Distorted Sign Board Detection using CNN with Optimal Resources*
Status: Finished

Stangl Jakob (M.Sc 2017, TU Wien)
Thesis Title: *Hardware acceleration of cryptographic procedures for secure distributed storage systems*
Status: Finished (**Awarded Best Master Thesis** at TU Wien)

Wess Matthias (M.Sc 2017, TU Wien)
Thesis Title: *Neural Network based ECG Anomaly Detection*
Status: Finished

Teaching Experience

2019 Fall 'VLSI Design for ASICs' course (Masters course at George Mason Univ.) - *Role:* Instructor

2018 Fall 'Applications of Metadata in Complex Big-Data Problems' course (Masters course at George Mason Univ.) - *Role:* Guest lecturer

2018 Fall 'Microprocessors' course (Masters course at George Mason Univ.) - *Role:* Guest lecturer

2018 Spring 'Advanced Microprocessors' course (Masters course at George Mason Univ.) - *Role:* Co-Instructor

2017 Fall Embedded Systems (Masters course at TU Wien, Austria) - *Role:* Instructor

2017 Spring Microcomputer Laboratory (Bachelors course at TU Wien) - *Role:* Instructor

2016 Fall Microcomputer Programming (Bachelors course at TU Wien) - *Role:* Instructor

2016 Spring Microcomputer Laboratory (Bachelors course at TU Wien) - *Role:* Instructor

2015 Fall Microcomputer Programming (Bachelors course at TU Wien) - *Role:* Instructor

Professional Service

2018-	TPC Member for GLSVLSI, ICCD, ESWEEK
2017-	TPC Member for IEEE PRIME, IEEE FDL
2017-	Reviewer for IEEE TMSCS, TCAD, TCSVT, ACM JETC
2016-	Reviewer for IEEE TCAS-I, TCAS-II, TVLSI, Elsevier VLSI Journal
2014, 2018-	External reviewer for Design Automation Conference

Accepted Publications Sorted by Topic [1]

Research Topic	Number of Publications
Machine learning (ML)	25
Hardware security	23 (**Two best paper award nominations**)
Big-data analytics	4
Resource management	14 (**One paper awarded with travel grant**)
Hardware for ML	13

Accepted Publications Sorted by Selected Conferences/Journals

Conference	Number of Publications
DATE	5
DAC	3
ICCAD	3
ESWEEK	3
IEEE Trans. on CAD	5
IEEE Trans. on Computers	2
IEEE Design & Test	2

[1] Some publications have overlap across multiple topics and some publications does not fit the area

List of Accepted Publications

[1] A. Vashist, A. Keats, **P. D. Sai Manoj**, and A. Ganguly. Securing a wireless network-on-chip against jamming based denial-of-service and eavesdropping attacks. *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, 2019. (Accepted), Impact factor (IF)=1.95.

[2] **P. D. Sai Manoj**, A. Joseph, A. Haridass, M. Shafique, J. Henkel, and H. Homayoun. Application and thermal reliability-aware reinforcement learning based multi-core power management. *ACM Transactions on Embedded Computing Systems*, 2019. (Accepted), Impact factor (IF)=1.36.

[3] **P. D. Sai Manoj**, A. Jantsch, and M. Shafique. Computer-aided arrhythmia diagnosis with bio-signal processing: A survey of trends and techniques. *ACM Computing Surveys*, 2018. (Accepted), IF=5.550.

[4] S. Pagani, **P. D. Sai Manoj**, A. Jantsch, and J. Henkel. Machine learning for power, energy, and thermal management on multi-core processors: A survey. *IEEE Transactions on Computer Aided Systems of Integrated Circuits and Systems*, 2018. (Accepted), IF=2.089.

[5] **P. D. Sai Manoj**, A. Jantsch, and M. Shafique. SmartDPM: Dynamic power management using machine learning for multi-core microprocessors. *Journal of Low-Power Electronics*, 14(4), Dec 2018. (Accepted), IF=0.840.

[6] M. Wess, **P. D. Sai Manoj**, and A. Jantsch. Weighted quantization-regularization in DNNs for weight memory minimization towards HW implementation. *IEEE Transactions on Computer Aided Systems of Integrated Circuits and Systems*, 2018. (Accepted), IF=2.089.

[7] **P. D. Sai Manoj**, J. Lin, S. Zhu, Y. Yin, X. Liu, X. Huang, C. Song, W. Zhang, M. Yan, Z. Yu, and H. Yu. A scalable network-on-chip microprocessor with 2.5D integrated memory and accelerator. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 64(6):1432–1443, June 2017. `https://ieeexplore.ieee.org/document/7819521/`, IF=2.823.

[8] D. Xu, N. Yu, H. Huang, **P. D. Sai Manoj**, and H. Yu. Q-learning based voltage-swing tuning and compensation for 2.5D memory-logic integration. *IEEE Design and Test*, 35(2):91–99, April 2018. http://ieeexplore.ieee.org/document/8070353/, IF=1.538.

[9] L. Ni, **P. D. Sai Manoj**, Y. Song, C. Gu, and H. Yu. A zonotoped macromodeling for eye-diagram verification of high-speed I/O links with jitter and parameter variations. *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 35(6):1040–1051, Jun. 2016. http://ieeexplore.ieee.org/document/7275122/, IF=2.089.

[10] D. Xu, N. Yu, **P. D. Sai Manoj**, K. Wang, H. Yu, and M. Yu. A 2.5-D memory-logic integration with data-pattern-aware memory controller. *IEEE Design Test*, 32(4):1–10, Aug. 2015. http://ieeexplore.ieee.org/document/7116522/, IF=1.538.

[11] **P. D. Sai Manoj**, H. Yu, H. Huang, and D. Xu. A Q-Learning based self-adaptive I/O communication for 2.5D integrated many-core microprocessor and memory. *IEEE Trans. on Computers*, 65(4):1185–1196, Apr. 2016. http://ieeexplore.ieee.org/document/7115114/, IF=3.052.

[12] **P. D. Sai Manoj**, H. Yu, and K. Wang. 3D many-core microprocessor power management by space-time multiplexing based demand-supply matching. *IEEE Trans. on Computers*, 64(11):3022–3036, Nov 2015. http://ieeexplore.ieee.org/document/7005482/, IF=3.052.

[13] Y. Song, H. Yu, and **P. D. Sai Manoj**. Reachability-based robustness verification and optimization of SRAM dynamic stability under process variations. *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 33(4):585–598, Apr. 2014. http://ieeexplore.ieee.org/document/6774560/, IF=2.089.

[14] **P. D. Sai Manoj**, H. Yu, Y. Shang, C. S. Tan, and S. K. Lim. Reliable 3-D clock-tree synthesis considering nonlinear capacitive TSV model with electrical-thermal-mechanical coupling. *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 32(11):1734–1747, Nov 2013. http://ieeexplore.ieee.org/document/6634568/, IF=2.089.

[15] H. Yu, L. Ni, and **P. D. Sai Manoj**. In *RRAM-based Machine Learning*. The IET, 2020. (In preparation).

[16] H. Yu, **P. D. Sai Manoj**, and H. Hantao. Cognitive I/O for 3D-integrated many-core system. In *Many core Computing: Hardware and Software*, chapter 19. The IET, 2019.

[17] Xiaojie Guo, Liang Zhao, Cameron Nowzari, Setareh Rafatirad, Houman Homayoun, and **P. D. Sai Manoj**. Deep multi-attributed graph translation with node-edge co-evolution. In *IEEE International Conference on Data Mining (ICDM) (**Accepted**)*, 2019.

[18] Abhijitt Dhavlle, Sahil Bhat, Setareh Rafatirad, Houman Homayoun, and **P. D. Sai Manoj**. Sequence-crafter: Side-channel entropy minimization as a defense for timing-based side-channel attack. In *ACM/IEEE International Conference on on Compilers, Architecture, and Synthesis for Embedded Systems (CASES) (**Accepted**)*, 2019.

[19] Rakibul Hassan, Setareh Rafatirad, Houman Homayoun, and **P. D. Sai Manoj**. Satconda: Sat to sat-hard clause translator. In *ACM/IEEE International Conference on on Compilers, Architecture, and Synthesis for Embedded Systems (CASES) (**Accepted**)*, 2019.

[20] Sanket Shukla, Gaurav Kolhe, **P. D. Sai Manoj**, and Setareh Rafatirad. Microarchitectural events and image processing-based hybrid approach for robust malware detection. In *ACM/IEEE International Conference on on Compilers, Architecture, and Synthesis for Embedded Systems (CASES) (**Accepted**)*, 2019.

[21] A. Vashist, A. Keats, **P. D. Sai Manoj**, and A. Ganguly. Unified testing and security framework for wireless network-on-chip enabled multi-core chips. In *ACM/IEEE International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS) (**Accepted**)*, 2019.

[22] Gaurav Kolhe, Hamid Mahmoodi, Avesta Sasan, **Sai Manoj PD**, Setareh Rafatirad, and Houman Homayoun. Security and complexity analysis of LUT-based obfuscation from blueprint to reality. In *ACM International Conference on Computer-Aided Design (**Accepted**)*, 2019.

[23] Hosein Mohammadi Makrani, Farnoud Farahmand, Hossein Sayadi, Sara Bondi, **Sai Manoj PD**, Setareh Rafatirad, and Houman Homayoun. Pyramid: Machine learning framework to estimate the optimal timing and resource usage of a high-level synthesis design. In *International Conference on Field-Programmable Logic and Applications (FPL) (**Accepted**)*, 2019.

[24] A. Vashist, A. Keats, **P. D. Sai Manoj**, and A. Ganguly. Securing a wireless network-on-chip against jamming based denial-of-service attacks. In *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, 2019.

[25] Gaurav Kolhe, **P. D. Sai Manoj**, Setareh Rafatirad, Hamid Mahmoodi, Avesta Sasan, and Houman Homayoun. On custom LUT-based obfuscation. In *ACM Great Lakes Symposium on VLSI*, 2019. `https://dl.acm.org/citation.cfm?id=3299874.3319496`.

[26] **P. D. Sai Manoj**, S. Amberkar, S. Bhat, A. Dhavlle, H. Sayadi, S. Rafatirad, and H. Homayoun. Adversarial attack on microarchitectural events based malware detectors. In *Design Automation Conference (DAC)*, 2019. `https://dl.acm.org/citation.cfm?id=3316781.3317762`.

[27] M. Taram, D. Tullsen, A. Venkat, H. Homayoun, and **P. D. Sai Manoj**. System security integration through hardware and firmware (SSITH). In *Government Microcircuit Applications and Critical Technology Conference (GOMACTech)*, 2019.

[28] **P. D. Sai Manoj**, H. Sayadi, H. Makrani, C. Nowzari, S. Rafatirad, and H. Homayoun. Lightweight node-level malware detection and network-level malware confinement in IoT networks. In *ACM/EDAA/IEEE Design Automation and Test in Europe (DATE)*, 2019. `https://ieeexplore.ieee.org/abstract/document/8715057`, (Acceptance rate=24.0%).

[29] H. Sayadi, H. Makrani, **P. D. Sai Manoj**, T. Mohsenin, A. Sasan, S. Rafatirad, and H. Homayoun. 2SMaRT: A two-stage machine learning-based approach for run-time specialized hardware-assisted malware detection. In *ACM/EDAA/IEEE Design Automation and Test in Europe (DATE)*, 2019. `https://ieeexplore.ieee.org/document/8715080`, (Acceptance rate=24.0%).

[30] **P. D. Sai Manoj**, S. Amberkar, S. Rafatirad, and H. Homayoun. Enhancing adversarial training towards robust machine learners and its analysis. In *International Conference on Computer-Aided Design (ICCAD)*, 2018. `https://ieeexplore.ieee.org/document/8587610`.

[31] M. Wess, **P. D. Sai Manoj**, and A. Jantsch. Weighted quantization-regularization in DNNs for weight memory minimization towards HW implementation. In *International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*, 2018. `https://ieeexplore.ieee.org/document/8412511`.

[32] **P. D. Sai Manoj**, Ferdinand Brasser, L. Davi, A. Dhavlle, T. Frassetto, S. Rafatirad, A. Sadeghi, A. Sasan, H. Sayadi, S. Zeitouni, and H. Homayoun. Advances and throwbacks in hardware-assisted security: Special session. In *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)*, 2018. `https://dl.acm.org/citation.cfm?id=3283552.3283567`.

[33] H.M. Makrani, H. Sayadi, **P. D. Sai Manoj**, S. Rafatirad, and H. Homayoun. A comprehensive memory analysis of data intensive workloads on server class architecture. In *International Symposium on Memory Subsystems*, 2018. `https://dl.acm.org/citation.cfm?id=3240320`.

[34] H.M. Makrani, H. Sayadi, **P. D. Sai Manoj**, S. Rafatirad, and H. Homayoun. Compressive sensing on storage data: An effective solution to alleviate I/O bottleneck in data-intensive workloads. In *IEEE International Conference on Application-specific Systems, Architectures and Processors*, 2018. `https://ieeexplore.ieee.org/document/8445131`.

[35] H. Sayadi, H.M. Makrani, O. Randive, **P. D. Sai Manoj**, S. Rafatirad, and H. Homayoun. Customized machine learning-based hardware-assisted malware detection in embedded devices. In *IEEE International Conference On Trust, Security And Privacy In Computing And Communications*, 2018.

[36] H. Sayadi, N. Patel, **P. D. Sai Manoj**, A. Sasan, S. Rafatirad, and H. Homayoun. Ensemble learning for effective run-time hardware-based malware detection: A comprehensive analysis and classification. In *ACM/EDAA/IEEE Design Automation Conference*, 2018. `https://dl.acm.org/citation.cfm?id=3196047`, (Acceptance rate=24.3%).

[37] H. Sayadi, **P. D. Sai Manoj**, A. Houmansadr, S. Rafatirad, and H. Homayoun. Comprehensive assessment of run-time hardware-supported malware detection using general and ensemble learning. In *ACM International Conference on Computing Frontiers*, 2018.

[38] **P. D. Sai Manoj** and A. Jantsch. ADDHard: arrhythmia detection with digital hardware by learning ECG signal. In *ACM Great Lakes Symposium on VLSI (GLSVLSI)*, 2018. `https://dl.acm.org/citation.cfm?id=3194647`.

[39] J. Stangl, T. Loruenser, and **P. D. Sai Manoj**. A fast and resource efficient FPGA implementation of secret sharing for storage applications. In *ACM/EDAA/IEEE Design Automation and Test in Europe (DATE) (**Nominated for Best Paper Award**)*, 2018. `https://www.date-conference.com/proceedings-archive/2018/html/bestpaper.html#b2` (Acceptance rate=24.1%).

[40] N. Taherinejad, A. Shami, and **P. D. Sai Manoj**. Self-aware sensing and attention-based data collection in multi-processor system-on-chips. In *IEEE New Circuits and Systems (NEWCAS)*, 2017. `http://ieeexplore.ieee.org/document/8010110/`.

[41] M. Wess, **P. D. Sai Manoj**, and A. Jantsch. Neural network based ECG anomaly detection on FPGA and trade-off analysis. In *International Symposium on Circuits and Systems (ISCAS)*, 2017. http://ieeexplore.ieee.org/document/8050805/.

[42] N. TaheriNejad, **P. D. Sai Manoj**, M. Rathmair, and A. Jantsch. Fully digital write-in scheme for multi-bit memristive storage. In *Conference on Electrical Engineering, Computing Science and Automatic Control*, Sep 2016. http://ieeexplore.ieee.org/document/7751193/.

[43] N. TaheriNejad, **P. D. Sai Manoj**, and A. Jantsch. Memristor's potential for multi-bit storage and pattern learning. In *European Modeling Symposium on Mathematical Modeling and Computer Simulation*, Oct 2015. http://ieeexplore.ieee.org/document/7579868/.

[44] J. Lin, S. Zhu, Z. Yu, D. Xu, **P. D. Sai Manoj**, and H. Yu. A scalable and reconfigurable 2.5D integrated multicore processor on silicon interposer. In *IEEE Custom Integrated Circuits Conf.*, pages 1–4, Sept 2015. http://ieeexplore.ieee.org/document/7338447/.

[45] **P. D. Sai Manoj**, K. Wang, H. Huang, and H. Yu. Smart I/Os: a data-pattern aware 2.5D interconnect with space-time multiplexing. In *ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, pages 1–6, June 2015. http://ieeexplore.ieee.org/document/7171707/.

[46] S. Ma, **P. D. Sai Manoj**, H. Yu, J. Ren, and R. Weerasekera. A 9.8 Gbps, 6.5 mW forwarded-clock receiver with phase interpolator and equalized current sampler in 65 nm CMOS. In *IEEE MTT-S International Microwave Symp.*, pages 1–4, May 2015. http://ieeexplore.ieee.org/document/7166838/.

[47] **P. D. Sai Manoj**, H. Yu, C. Gu, and C. Zhuo. A zonotoped macromodeling for reachability verification of eye-diagram in high-speed I/O links with jitter. In *2014 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pages 696–701, Nov 2014. http://ieeexplore.ieee.org/document/7001428/ (Acceptance rate=25.0%).

[48] H. Hantao, **P. D. Sai Manoj**, D. Xu, H. Yu, and Z. Hao. Reinforcement learning based self-adaptive voltage-swing adjustment of 2.5D I/Os for many-core microprocessor and memory communication. In *IEEE/ACM Int. Conf. on Computer-Aided Design (ICCAD)*, pages 224–229, Nov 2014. http://ieeexplore.ieee.org/document/7001356/ (Acceptance rate=25.0%).

[49] D. Xu, **P. D. Sai Manoj**, H. Huang, N. Yu, and H. Yu. An energy-efficient 2.5D through-silicon interposer I/O with self-adaptive adjustment of output-voltage swing. In *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, pages 93–98, Aug 2014. http://ieeexplore.ieee.org/document/7298229/.

[50] S. S. Wu, K. Wang, **P. D. Sai Manoj**, T. Y. Ho, M. Yu, and H. Yu. A thermal resilient integration of many-core microprocessors and main memory by 2.5D TSI I/Os. In *Design, Automation Test in Europe Conference Exhibition (DATE)*, pages 1–4, March 2014. http://ieeexplore.ieee.org/document/6800391/ (Acceptance rate=23.1%).

[51] Y. Song, **P. D. Sai Manoj**, and H. Yu. Zonotope-based nonlinear model order reduction for fast performance bound analysis of analog circuits with multiple-interval-valued parameter variations. In *Design, Automation Test in Europe Conference Exhibition (DATE)*, pages 1–6, March 2014. http://ieeexplore.ieee.org/document/6800225/ (Acceptance rate=23.1%).

[52] Y. Song, **P. D. Sai Manoj**, and H. Yu. A robustness optimization of SRAM dynamic stability by sensitivity-based reachability analysis. In *Asia and South Pacific Design Automation Conference (ASP-DAC)*, pages 461–466, Jan 2014. http://ieeexplore.ieee.org/document/6742934/.

[53] J. Wang, S. Ma, **P. D. Sai Manoj**, M. Yu, R. Weerasekera, and H. Yu. High-speed and low-power 2.5D I/O circuits for memory-logic-integration by through-silicon interposer. In *IEEE International 3D Systems Integration Conference (3DIC)*, pages 1–4, Oct 2013. http://ieeexplore.ieee.org/document/6702326/.

[54] P. D. Sai Manoj, K. Wang, and H. Yu. Peak power reduction and workload balancing by space-time multiplexing based demand-supply matching for 3D thousand-core microprocessor. In *ACM/EDAC/IEEE Design Automation Conf.*, pages 1–6, May 2013. http://ieeexplore.ieee.org/document/6560768/ (Acceptance rate=21.7%).

[55] Y. Song, H. Yu, **P. D. Sai Manoj**, and G. Shi. SRAM dynamic stability verification by reachability analysis with consideration of threshold voltage variation. In *ACM International Symposium on International Symposium on Physical Design*, pages 43–49, 2013. http://dl.acm.org/citation.cfm?id=2451927.

[56] **P. D. Sai Manoj** and H. Yu. Cyber-physical management for heterogeneously integrated 3D thousand-core on-chip microprocessor. In *IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 533–536, May 2013. http://ieeexplore.ieee.org/document/6571898/.