Lecture 4

Carry-Skip, Carry-Select, & Conditional-Sum Adders

Fixed-Block-Size Carry-Skip Adder (1)

Notation & Assumptions

Adder size - k-bits
Fixed block size - b bits
Number of stages - t

Delay of skip logic = Delay of one stage of ripple-carry adder
= 1 delay unit

Latency of the carry-skip adder with fixed block width

$$\text{Latency}_{\text{fixed-carry-skip}} = \underbrace{(b-1)}_{\text{in block 0}} + \underbrace{0.5}_{\text{OR gate}} + \underbrace{\frac{k}{b} - 2}_{\text{skips}} + \underbrace{(b-1)}_{\text{in last block}}$$

$$= 2b + \frac{k}{b} - 3.5$$

Fixed-Block-Size Carry-Skip Adder (2)

Optimal fixed block size

$$\frac{dLatency_{fixed\text{-}carry\text{-}skip}}{db} = 2 - \frac{k}{b^2} = 0$$

$$b_{opt} = \sqrt{\frac{k}{2}} \qquad t_{opt} = \left\lceil \frac{k}{b_{opt}} \right\rceil = \sqrt{2k}$$

$$Latency^{opt}_{fixed\text{-}carry\text{-}skip} = 2\sqrt{\frac{k}{2}} + \frac{k}{\sqrt{\frac{k}{2}}} - 3.5 =$$

$$= \sqrt{2k} + \sqrt{2k} - 3.5 = \boxed{2\sqrt{2k} - 3.5}$$

Fixed-Block-Size Carry-Skip Adder (3)

k	b_{opt}	t_{opt}	$Latency_{fixed\text{-}carry\text{-}skip}$	$Latency_{ripple\text{-}carry}$	$Latency_{look\text{-}ahead}$
32	4	8	12.5	32	6.5
128	8	16	28.5	128	8.5
16	2	8	8.5	16	4.5
	3	5	7.5		
64	5	13	18.5	64	6.5
	6	11	18.5		

Variable-Block-Size Carry-Skip Adder (1)

Notation & Assumptions

Adder size - k-bits

Number of stages - t

Block size - variable

First and last block size - b bits

Delay of skip logic = Delay of one stage of ripple-carry adder
= 1 delay unit

Variable-Block-Size Carry-Skip Adder (2)

Optimum block sizes

b_{t-1} b_{t-2} b_{t-3} . . . $b_{t/2+1}$ $b_{t/2-1}$ . . . b_2 b_1 b_0

b b+1 b+2 . . . $b+\frac{t}{2}-1$ $b+\frac{t}{2}-1$ b+2 b+1 b

Total number of bits

$$k = 2\,[\, b + (b+1) + (b+2) + \ldots + (b + \frac{t}{2} + 1\,)\,] =$$

$$= t\,(\, b + \frac{t}{4} - \frac{1}{2}\,)$$

Variable-Block-Size Carry-Skip Adder (3)

Number of bits in the first and last block

$$b = \frac{k}{t} - \frac{t}{4} + \frac{1}{2}$$

Latency of the carry-skip adder with variable block width

$$\text{Latency}_{\text{fixed-carry-skip}} = \underbrace{(b-1)}_{\text{in block 0}} + \underbrace{0.5}_{\text{OR gate}} + \underbrace{t-2}_{\text{skips}} + \underbrace{(b-1)}_{\text{in last block}}$$

$$= 2b + t - 3.5 = 2\left(\frac{k}{t} - \frac{t}{4} + \frac{1}{2}\right) + t - 3.5 =$$

$$= \frac{2k}{t} + \frac{1}{2}t - 2.5$$

Variable-Block-Size Carry-Skip Adder (4)

Optimal number of blocks

$$\frac{d\text{Latency}_{\text{variable-carry-skip}}}{dt} = -\frac{2k}{t^2} + \frac{1}{2} = 0$$

$$\Rightarrow \quad t_{opt} = \sqrt{4k} = 2\sqrt{k}$$

$$b_{opt} = \frac{k}{t_{opt}} - \frac{t_{opt}}{4} + \frac{1}{2} =$$

$$= \frac{k}{2\sqrt{k}} - \frac{2\sqrt{k}}{4} + \frac{1}{2} = \frac{1}{2}$$

$$\Rightarrow \quad b_{opt} = 1$$

Variable-Block-Size Carry-Skip Adder (5)

Optimal latency

$$\text{Latency}^{\text{opt}}_{\text{variable-carry-skip}} = \frac{2k}{t} + \frac{1}{2}t - 2.5 =$$

$$= \frac{2k}{2\sqrt{k}} + \frac{2\sqrt{k}}{2} - 2.5 =$$

$$= 2\sqrt{k} - 2.5$$

$$\text{Latency}^{\text{opt}}_{\text{variable-carry-skip}} \approx \frac{\text{Latency}^{\text{opt}}_{\text{fixed-carry-skip}}}{\sqrt{2}}$$

Multilevel Carry-Skip Adders (1)

Notation & Assumptions

Adder size - k-bits

Number of stages - t

1 delay unit =

Generation of g_i and p_i signals =
Generation of a level i skip signal from level (i-1) signals
Delay of one stage of ripple-carry adder =
Delay of skip logic =
Delay of sum logic

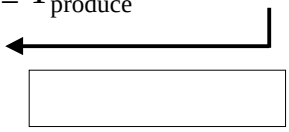
Delay of a single OR gate proceeding the first skip neglected

Multilevel Carry-Skip Adders (2)

$\{ T_{produce}, T_{assimilate} \}$

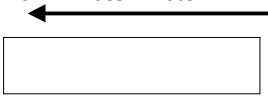
time = 0 $T_{produce} = \beta$

time $\leq T_{produce}$



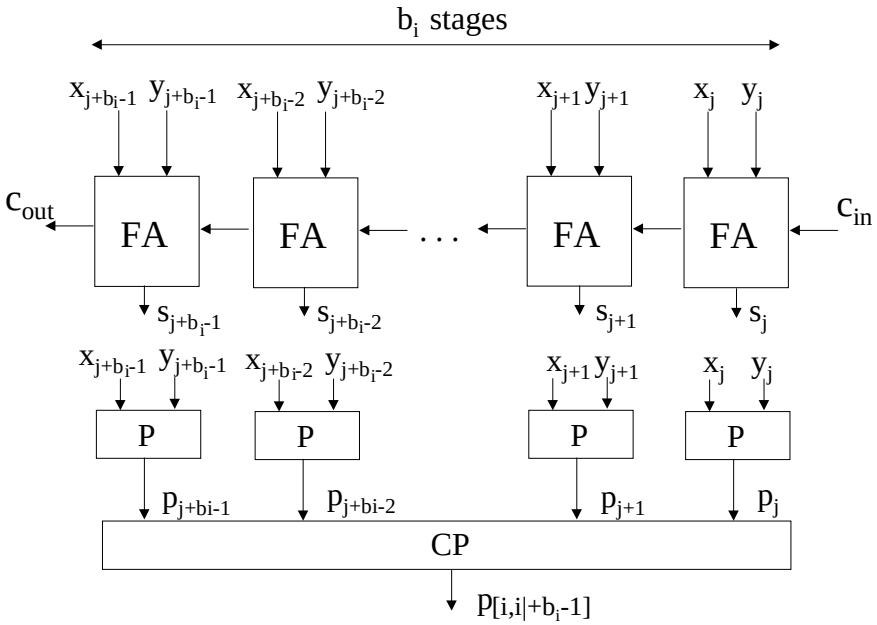
carry out generated by a given block must appear at the output no later than $T_{produce}$

time $\leq t_0 + T_{assimilate}$ time = t_0 $T_{assimilate} = \alpha$

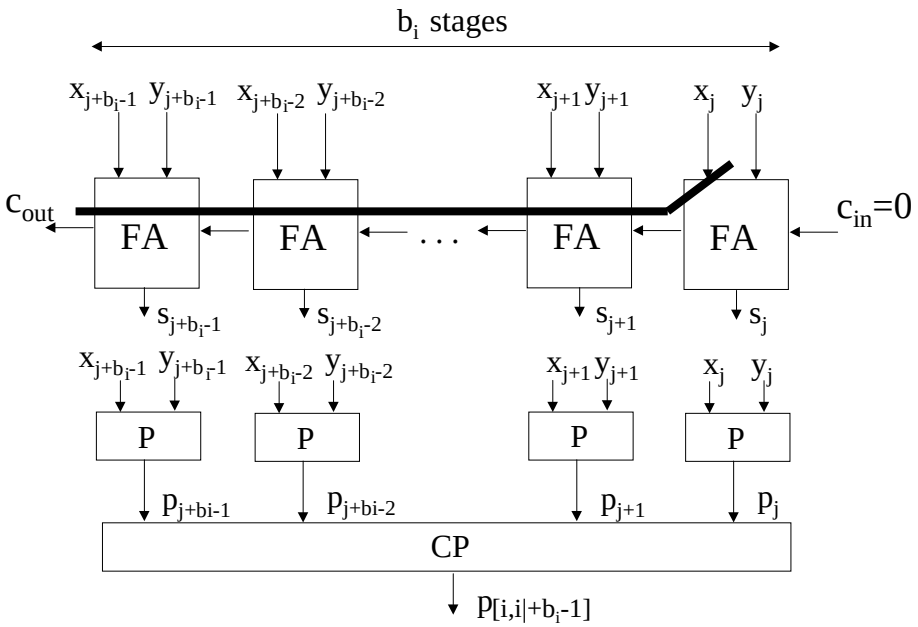


Time to propagate within a block should not exceed $T_{assimilate}$

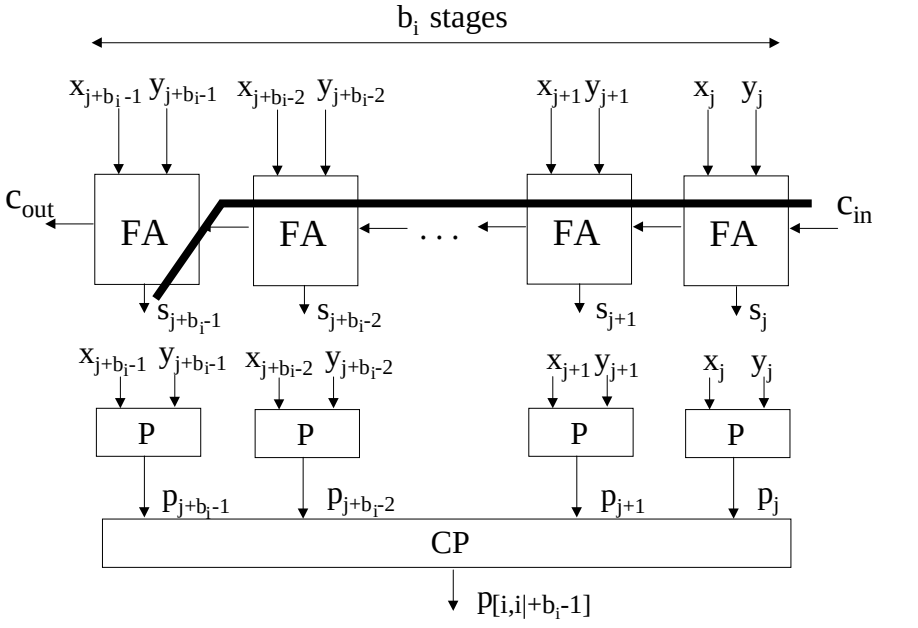
Single block of carry-skip adder



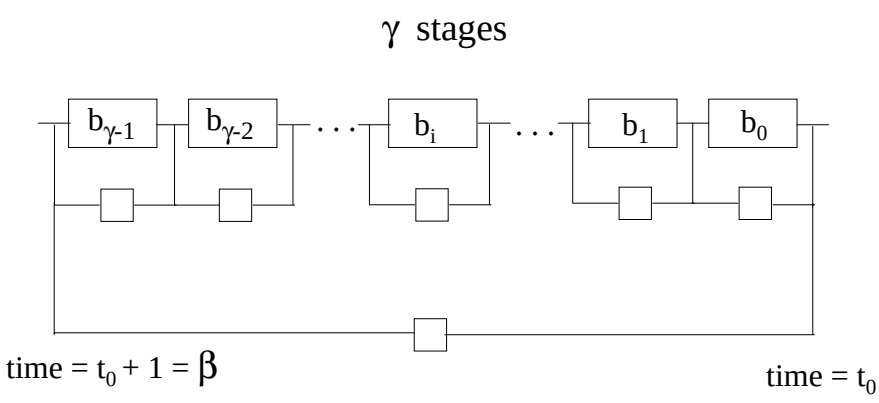
Most critical path to produce carry



Most critical path to assimilate carry



Multilevel Carry-Skip Adders (3)



Multilevel Carry-Skip Adders (4)

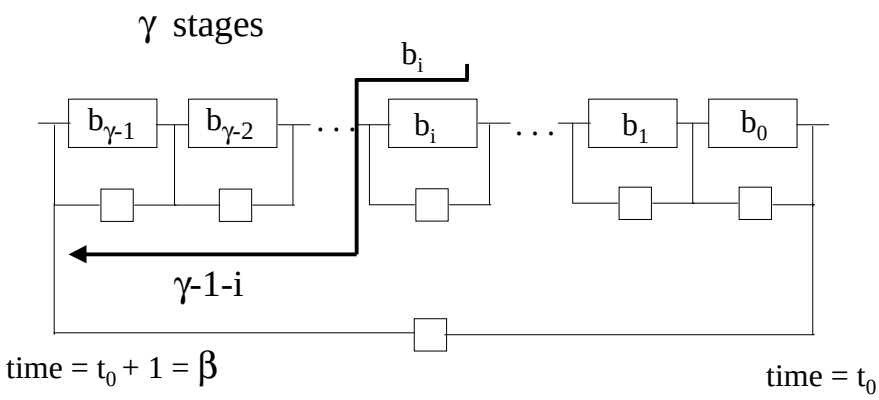
Number of first level subblocks

$$\gamma = \min (\beta - 1, \alpha)$$

Width of the i-th subblock

$$b_i = \min (\beta - \gamma + i + 1, \alpha - i)$$

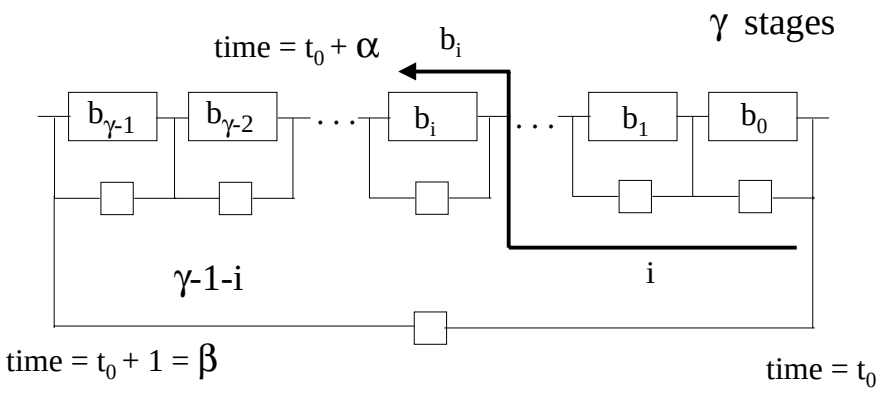
Multilevel Carry-Skip Adders (5)



$$b_i + (\gamma - 1 - i) \leq \beta$$

$$b_i \leq \beta - \gamma + i + 1$$

Multilevel Carry-Skip Adders (6)



$$b_i + i \leq \alpha$$

$$b_i \leq \alpha - i$$