Project 2 Specification
64-bit Signed Multiplier-Accumulator (MAC)
April 1, 2002
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1. Functional Requirement:

A 64-bit signed multiplier-accumulator (MAC) shall be designed to operate on either one or two sequences of signed 64-bit numbers. If time permits, the MAC shall be modified to operate on two complex numbers $\{x_i = a + jb, y_i = c + jd\}$(see pg. 162 of "The Designer's Guide to VHDL", by Peter J. Ashenden). The MAC shall multiply and add the sequences of numbers according the equation below where N is the length of the sequences:

$$\sum_{i=1}^{N} x_i y_i$$

The complex numbers and their sum shall be calculated as follows:

$Product_{real} = ac – bd$
$Product_{imaginary} = ad + bc$

$Sum_{real} = a + c$
$Sum_{imaginary} = b + d$

Finally, the MAC shall be capable of accumulating up to 256 partial products, permit parallel read-out of the sum, and be optimized for maximum throughput.

2. Application:

MAC's that perform multiplications on a stream of complex numbers are used in many digital signal processing applications such as digital demodulation and filtering and equalization.

3. The MAC shall utilize a pipelined architecture illustrated in Fig. 1 and Fig. 2 to maximize the throughput of the MAC. The multiplier and accumulator blocks will consist of a right-shift multiplier and carry-lookahead adder respectively.

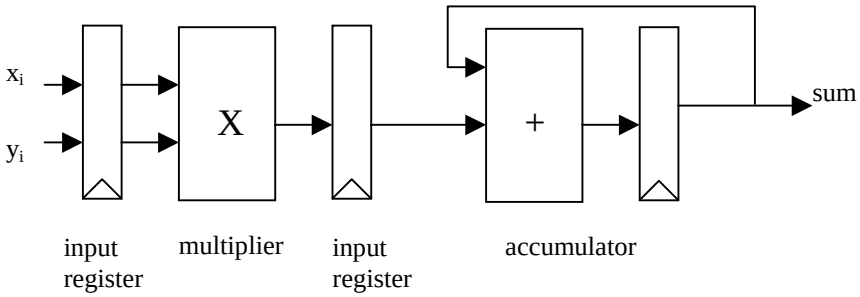

Figure 1. MAC for Two Signed 64-bit Numbers

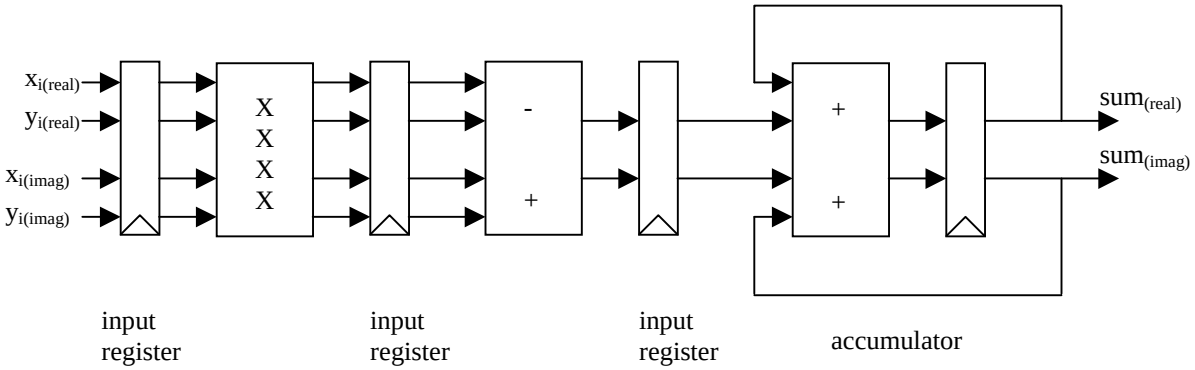

Figure 2. MAC for Two 64-Bit Signed Complex Numbers

4. Computer aided design (CAD) tools:

The following CAD tools (available in the ECE labs) shall be used in the MAC design:

VHDL simulator and compiler: ModelSim SE, Version 5.5e
Logic Synthesis: Leonardo Spectrum, Version: v2001_1d.46