PROJECT 2 SPECIFICATIONS

As planning to concentrate mostly on the hardware part as suggested in the project2, software specifications are not mentioned in full

A. NAMES OF THE TEAM MEMBERS:

1. Purnachander Mangu
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B. TITLE OF THE PROJECT:

Topic 3:
1. Multiplication of two 64-bit signed numbers and division of a 128-bit number by a 64-bit number

C. HARDWARE AND SOFTWARE UNIT INITIAL SPECIFICZTIONS:

1. Functional requirements of hardware:
   - Arithmetic Operations:
     - $C = A \cdot B$
     - $C = A/B$
   - Number and sizes of operands:
     - Inputs (A, B): std_logic_vector (0 to 63) 64-bit size for hardware
       : Signed double or signed long double for Software
     - Output (C): std_logic_vector (0 to 63) 64-bit size for hardware
       : double or long double for software
     - Some of the temporary signals may be of 128-bit size
   - Control signals for HW and function arguments for SW:
     - Standard logic vector inputs (A, B) and standard logic vector output (C) from ieee_1164 std_logic library
     - A, B: signed double/long double, C: signed double/ long double and some of the intermediary signals are of type long double

2. Example of a real life application:
   Used in the arithmetic and logic unit of a general-purpose microprocessor. Addition and subtractions are the basic operations in arithmetic and logic units, multiplication and division are then extended depending on the architecture. Whenever an ALU is designed it is important that it should contain all the information of size of the operands and specific operations performed.

3. Optimization criteria:
    HW
    ➢ Minimum Latency
    ➢ Maximum throughput
    ➢ Limited area
    SW
    ➢ Minimum execution time
    ➢ Limited memory

4. CAD Tools:
    ➢ Hardware Tools:
        o Aldec Active HDL (Version 4.1) using at home on Windows XP®
        o Mentor Graphics Model Sim (version 5.4) using in ECE FPGA lab (ST II, Room203), which is being operated under Solaris Environment
        o Cadence Pspice Capture for circuit or gate level simulation using in ECE lab (ST II, Room265)
    ➢ Software Tools:
        o C/C++ Compiler at School
        o Visual C++ (Visual Studio) at home.

5. Assumptions:
    ➢ For HW:
        o Elementary components planning to consider are: Full adder, Multiplexer, and some behavioral procedures for complementing and so on.
        o All the components will be designed using appropriate gates and it is assumed that the delay of all the gates will be equal. Their area is approximated depending on the transistor occupancy (estimated using Pspice)
    ➢ For SW:
        o Planning to use 'C'.
        o Basic library function that are planning to be used are logical functions like shifting, some of the arithmetic functions such as complementing and also conditional statements

6. Test Plan:
    ➢ For HW:
        o A test bench will be written using which the test vectors will be passed through the main module and tested for its functionality.
        o The circuit speed will be determined depending on the gate levels used and using some time dependant execution functions.
        o The circuit area will be determined with the help of Pspice and manual estimation of gates used.

- For SW:
  - Run time test vectors are used to determine the functionality of the software code written
  - Function execution time will be calculated using some of the library functions, which calculates the time taken by the processor for that particular operation.
  - Values of the operands used for functional and timing verification are similar except stressing a particular function.
7. List of references:
   - For HW:
     - Computer Arithmetic: Hardware and software implementation by Behrooz Perhami.
     - Computer Arithmetic by Isreal Koren
     - Micro processor Architecture by Douglas Hall
     - "http://www.wlu.ca/~wwwphys/People/nznotina/cp464/datasheets/74181.pdf"
   - For SW:
     - The C programming Language by B.Kernighan & D. Ritchie
     - C/C++ Bible
     - Let us C by Yashwanth kantkar.