ECE 645: PROJECT SPECIFICATION

TITLE: A VHDL Implementation of a 3-D Cross-Correlator for Template Matching

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Date: 4/12/02

1. Functional Requirement

The design will implement the cross-correlation algorithm given below.

$$R(x,y,z) = \sum_{i=0}^{m} \sum_{j=0}^{n} \sum_{k=0}^{p} f(x+m, y+n, z+p) * g(m,n,p)$$

Where the template is given by g(x,y,z) and the area over which the template is to be matched is given by the function defined by the function f. The algorithm involves iterating the template over the input data values with the maximum value of R(x, y, z) giving the best match. This algorithm is well suited for the implementation of a MAC. The size of the template to be matched is g(8,11,10) and the input data consists of an area of size f(24,11,416), where each of the specified points consist of 16-bit unsigned binary numbers.

2. Application

The above algorithm is used extensively for automatic target recognition in DSP applications. More specifically this implementation will be used for automatic target recognition of landmines.

3. Optimization Criteria

This design is part of an ongoing research into an optimal architecture for a 3-D cross-correlator. Initial goals are based on conflicting requirements of optimal throughput for real-time applications and minimum chip area for a cost effective design. The initial design will be based on an architecture that can be implemented on the SLAAC1-V board with maximum area utilization to achieve optimal throughput for real time applications.

4. Design Tools

The design will be done in VHDL. Simulation will be done using Active HDL. The synthesis tool will be the Xilinx ISE FPGA Express.

5. Assumptions

The target device will be the SLAAC1-V board, which consists of three Virtex1000 chips. The board also has ten 36 x 256K ZBT SRAMs ideal for the large amounts of data that need to be processed.

The variation of the energy of the image f can be ignored, thus a normalized version of the algorithm does not need to be implemented.

6. Test Plan

The active HDL tool will be used to simulate and test the functionality of the design based on data collected using a Ground Penetrating Radar over various calibration lanes containing deactivated landmines.

Actual circuit speed and area determined by the synthesis results will determine what optimization criteria will take priority. Since the primary concern for this project is for a cost effective design, the goals of area and speed optimizations depend largely the results obtained from a crude design since the primary criteria for a cost effective design involves production time.

7. References

1. Andrew Rushton, "VHDL for Logic Synthesis," 2nd Edition, John Wiley and Sons Ltd, West Sussex PO19 1UD, England 1998

2. I. Koren, "Computer Arithmetic Algorithms," 2nd edition, A K Peters Ltd., Massachusetts 2000.

3. Xilinx website (Virtex documentation); http://www.xilinx.com/

4. Ashenden, Peter J., "The designers guide to VHDL," San Francisco: Morgan Kaufman, 1996

5. There are currently no references to a hardware implementation of a 3-D cross-correlator for template matching.