

Midterm exam II
20 points total

Part I

1. **(2 point)** Determine all bits of the ANSI/IEEE standard single-precision representation of the following numbers:
 - a. -156.46875_{10}
 - b. $0.01111011_2 \cdot 2^{-127}$

2. **(3 points)** Multiply the following two 8-bit numbers using radix-4 multiplication with Booth's recoding. Show all intermediate operands and partial products in the binary notation.
$$a = -112_{10}$$
$$x = 123_{10}$$

3. **(2 points)** Arrange the following 7-bit multipliers in the order of increasing latency. Assume that all components are built of NOT, AND, OR, and XOR gates and D flip-flops. The delays of all gates and the delay of a D-flip-flop are equal to one time unit, and the D-flip-flop setup time is equal to 0.5 time unit.
 - a. binary multiplier with left shifts (*Parhami*, Fig. 9.6)
 - b. binary multiplier with right shifts using carry save adders (*Parhami*, Fig. 10.8)
 - c. radix-4 multiplier with the cumulative partial product (*Parhami*, Fig. 10.11)
 - d. Wallace tree multiplier (*Parhami*, Fig. 11.3)
 - e. serial systolic multiplier (*Parhami*, Fig. 12.10)

4. **(3 points)** Determine the ratio of areas of an 8x8 bit multiplier and an 8-bit squarer built of NAND gates and optimized for minimum latency.

Part II (5 points for each problem)

1. Design a 5x5 bit unsigned multiplier optimized for the minimum possible latency. Assume that the multiplier is built of NAND gates only. Compute the circuit latency.

2. Estimate the latency of the radix-2 divider with partial remainder stored in carry-save form shown in *Parhami*, Fig. 14.8, assuming that all components are built of NOT, AND, OR, and XOR gates and D flip-flops. The delays of all gates and the delay of a D-flip-flop are equal to one time unit, and the D-flip-flop setup time is equal to 0.5 time unit. Describe all assumptions you make.