

Midterm exam I
20 points total

April 5, 2000

Part I

1. **(1 point)** Match the following 6-bit representations of -21 with the names of these representations:

- A. 101010
- B. 110101
- C. 001011
- D. 101011

- a. biased with $B=2^5$
- b. one's complement
- c. two's complement
- d. signed magnitude

2. **(2 points)** Arrange the following signals in the order they are generated within the 64-bit 3-level carry lookahead adder shown in *Parhami*, Fig. 6.5, starting from the signal that is generated first. Assume that the adder is built of AND, OR, and XOR gates, and that delays of all these gates are equal.

- A. p_{63}
- B. s_8
- C. $g_{[48, 51]}$
- D. c_{57}
- E. s_{32}

3. **(2 points)** Arrange the following numbers in the ascending order:

- A. $(2E.A)_{16}$
- B. $(166.25)_{-10}$
- C. $(1 -2 1 -2)_4$
- D. $(57.64)_{1/10}$
- E. $(1 1 1 -1 -1 -1 1)_2$

4. **(2 points)** Arrange the following 64-bit adders in the order of increasing worst case delay. Assume that all adders are built of AND, OR, and XOR gates, and that the delays of all these gates are equal. Every adder accepts carry-in and produces carry-out.
- A. ripple-carry adder
 - B. 1-level carry-skip adder with 8-bit skip blocks
 - C. 2-level carry-select adder based on shorter ripple-carry adders
 - D. 3-level carry-lookahead adder
5. **(1 point)** Determine the longest path carry propagates through during the addition of the following two 16-bit numbers. Your answer should include the bit position where the carry is generated, and the bit position where the carry is annihilated.

0111 0110 1101 1011
0101 1001 1010 1011

6. **(2 points)** Using dot notation, show addition of eight 4-bit numbers in the Wallace tree.

Part II (4 points for each problem)

1. Design an 8-bit adder using the following components: 8-input Brent-Kung parallel prefix network built of NAND gates, supplemented with additional NAND gates. Estimate the delay and area of this adder expressed in the number of gate levels and the number of NAND gates respectively.
2. Build an optimum fixed-block-size one-level 64-bit carry-skip adder. Assume that ripple and skip delays are equal to one time unit.
3. Design a minimum-latency 16-bit decremter, built of AND, OR, and XOR gates. Estimate the delay and area of this decremter expressed in the number of gate levels and the number of gates respectively.