

ECE 699—Digital Signal Processing Hardware Implementations
Department of Electrical and Computer Engineering
George Mason University
Spring 2009

Lectures: Wednesday, 4:30 - 7:10 PM, Robinson Hall, Room B208
Hands-on sessions may be held periodically during class hours in ST2, Room 203.

Web Page: <http://mason.gmu.edu/~dhwang/ece699/spring2009/>

Instructor: Dr. David Hwang
Email: dhwang@gmu.edu
Office Hours: Monday, 4:30 – 5:30 pm, ST2, Room 229
Thursday, 4:30 – 5:30 pm, ST2, Room 229

Course Description

This graduate course will investigate implementations of digital signal processing algorithms in hardware (including FPGAs and ASICs) and will discuss the use of DSP hardware in modern applications such as mobile phones and wireless LAN. Specifically, the course will investigate:

- 1) High-level DSP optimizations such as pipelining, unfolding, and parallel processing
- 2) Common DSP structures such as pipeline FFTs, finite impulse response (FIR) filters, direct digital frequency synthesizers, and correlators
- 3) Modeling of DSP algorithms in Matlab and conversion of Matlab models into fixed-point VHDL blocks
- 4) Platform implementation issues: hardware vs. software, FPGA vs. ASIC, power, area, throughput, etc.
- 5) Applications of DSP hardware such as mobile phones, satellite receivers, and software defined radios

Prerequisites

- 1) ECE 545, or a demonstrated proficiency with synthesizable VHDL and the Xilinx FPGA flow
- 2) Undergraduate-level understanding of digital signal processing and Matlab

Required Textbook

Keshab K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*, Wiley, 1999, ISBN: 978-0471241867.

Supplementary Textbooks

Uwe Meyer-Baese, *Digital Signal Processing with Field Programmable Gate Arrays*, 3rd Edition, Springer, 2007, ISBN: 978-3540726128.

VHDL refresher textbook

Volnei A. Pedroni, *Circuit Design with VHDL*, The MIT Press, 2004, ISBN: 0-262-16224-5.

DSP refresher textbooks

John G. Proakis and Dimitris K. Manolakis, *Digital Signal Processing: Principles, Algorithms, and Applications*, 4th edition, Prentice Hall, 2006, ISBN: 978-0131873742. [3rd edition also fine]

Alan V. Oppenheim, Ronald W. Schaffer, and John R. Buck, *Discrete-Time Signal Processing*, 2nd edition, Prentice Hall, 1999, ISBN: 978-0137549207.

Communication

Communication will be made from the instructor via email and the course web page. I will send emails to your official GMU email account; be sure to check this regularly or forward your GMU mail to an account you check regularly. Lectures will be posted on the web page for download by 12 noon on the day of class. Please check the web page regularly for course updates and announcements.

Grading

Your course grade will be determined by a combination of homework, presentation, midterm, and final:

Presentation	15%
Homework	20%
Midterm Exam	30%
Final Exam	35%

Schedule

A preliminary schedule is below; modifications to lecture topics may be made. The schedule on the course website will contain up-to-change modifications.

Wed, Jan 21	Lecture 1 - Introduction, Fixed-Point Arithmetic (1)
Wed, Jan 28	Lecture 2 - Fixed-Point Arithmetic (2), FIR Filters and Pipelining (1)
Wed, Feb 4	Lecture 3 - FIR Filters and Pipelining (2)
Wed, Feb 11	Lecture 4 - DSP-Specific Hardware in FPGAs
Wed, Feb 18	Lecture 5 - IIR Filters, Iteration Bound
Wed, Feb 25	Lecture 6 - Fast Fourier Transforms
Wed, Mar 4	Lecture 7 - CORDIC, Direct Digital Frequency Synthesizers
Wed, Mar 11	NO CLASS - SPRING BREAK
Wed, Mar 18	Lecture 8 - Bit-Level DSP Arithmetic (1), Midterm Review
Wed, Mar 25	MIDTERM EXAM
Wed, Apr 1	Lecture 9 - Bit-Level DSP Arithmetic (2)
Wed, Apr 8	Lecture 10 - Retiming Transformations
Wed, Apr 15	Lecture 11 - Folding/Unfolding Transformations
Wed, Apr 22	Lecture 12 - Advanced Topics, Final Review
Wed, Apr 29	Lecture 13 - Student Presentations
Wed, May 6	FINAL EXAM

Attendance

There is no explicit attendance requirement, but students are expected to attend all courses. If you are absent, you are responsible for turning homework on time and obtaining class notes from another student.

Homework

Students are required to submit all homework assignments. No late homework will be accepted. Homework assignments are to be completed individually.

Presentation

Students will work in groups to two to present a presentation on a DSP hardware topic. The list of topics will be given by the instructor during the course of the semester.

Students with Disabilities

Please talk with me to make arrangements to accommodate your needs.

Honor Code

All rules of the GMU Honor Code system will be in effect. All students should be familiar with the code and abide by its rules. Cheating is taken very seriously. If you violate the honor code, you will be reported to the honor committee and may face sanctions ranging from an F in the course to expulsion from GMU. The honor code (<http://www.gmu.edu/catalog/apolicies/#Anchor13>) states:

Student members of the George Mason University community pledge not to cheat, plagiarize, steal, or lie in matters related to academic work.