

GMU ECE 699—Digital Signal Processing Hardware Architectures Spring 2009 Project Presentations

Wednesday, April 29, 2009, 4:30 pm – 7:45 pm
Student Union Building II (SUB II), Room 4

NOTE: Each session will count as one seminar credit (unless you are a presenter in the session).

SESSION 1—DSP Software Techniques

- 4:30 – 4:45 Texas Instruments Programmable DSP Processors and Design Environment
Thuy-Tien Nguyen and Anne-Marie Cressin
- 4:45 – 5:00 Analog Devices Programmable DSP Processors and Design Environment
Dawit Adane and Mark Adam
- 5:00 – 5:15 High-level Synthesis CAD Tools -- Conversion from C to RTL
Ekawat Homsirikamol and Venkata Amirineni
- 5:15 – 5:25 BREAK

SESSION 2—FPGA DSP Architectures

- 5:25 – 5:40 Bit-serial DSP architectures on FPGAs
Joseph Burns and Xung Nham
- 5:40 – 5:55 Floating-Point Digital Signal Processing on FPGAs
James Northern
- 5:55 – 6:10 Multi-Rate Digital Signal Processing on FPGAs
Arvind Bhat and Shan Chiang
- 6:10 – 6:25 Self-Adaptive Filters on FPGAs
Xin Xin and Shaunak Shah
- 6:25 – 6:35 BREAK

SESSION 3—FPGA Platforms

- 6:35 – 6:50 Software-Defined Radio Platforms (FPGAs + DSPs)
Mark Chaney and Jeremy Kelly
- 6:50 – 7:05 DSP-specific blocks on Actel FPGAs
Matthew Williams and Alberto Villareal
- 7:05 – 7:20 DSP-specific blocks on Altera FPGAs
Greg Zumbrook and Ian Cyr
- 7:20 – 7:35 Xilinx System Generator and AccelDSP
Nikita Charankar and Abirami Prabhakaran