

**ECE 545 Fall 2008**  
**Synthesis and Implementation**

**Option 1: Aldec Environment (School)**

VHDL Simulator: Aldec Active-HDL (7.2 SP2)

Synthesis: Synplicity Synplify Pro (8.6.2) or Xilinx ISE Foundation XST (ISE 9.1 SP3)

Implementation: Xilinx ISE Foundation (ISE 9.1 SP3)

**Synthesis:**

(\* Make sure all your design files are compiled.

(\* Go to the design flow window and select <options> above the synthesis box, then to the left hand side corner you will see design files listed out ranked. Unless specified the hierarchy will be in the order your files are compiled. If not, push the "Update synthesis order" button on the bottom and it should update your synthesis order to match your compilation order. It should be from lowest to highest hierarchy.

(\* Remove the testbench from your synthesis order (Right click and unselect "Include in synthesis"). Note: Testbench should not be included in synthesis.

(\* Under general tab select the top level unit as your main source code, select the FPGA family <Xilinx9x SPARTAN3 or specified>, device <smallest or required size> and speed grade <fastest> from the push down list.

(\*Run the synthesis in <batch mode> (Synplicity only); select the simulation output format as <VHDL>. By Default the frequency you run will be <Autoconstrain> but if you want to request your own frequency go to <settings> and unselect <Autoconstrain> and specify the required frequency. Also select view mode as <RTL> (Synplicity only).

(\* Single click on <synthesis>. It shows up as a dialog wizard with synthesis running, if you wish to terminate the synthesis before it ends select <abort> at the bottom. Once synthesis is done, click <close> at the bottom.

(\* You may get a warning about DSP48. This is okay.

(\* To view the synthesis report select <reports> below the synthesis box.

**Post-synthesis simulation:**

(\* Select <options> below post synthesis simulation box, under <general>,<input files> by default you will have a .vhm file generated from synthesis (for Synplicity) or a .vhd file generate from synthesis (for XST).

(\*) Add the testbench to your input files.

(\*) Select top level unit as <Testbench>

(\*) You may have to modify your testbench vhd file to comment out references to generic mapping. Comment out generic ports in the component declaration and generic port maps in the component instantiation. Then recompile the testbench ONLY. After synthesis the top-level entity will not have generic ports any longer.

(\*) Single click on <post-synthesis simulation>. observe the waveform and save it. Note the waveform does not have any propagation delay information (i.e. it should look the same as your pre-synthesis simulation).

### **RTL mode (Synplicity Only):**

(\*)To view the schematic diagram of your design single click on RTL view. This will open Synplicity.

(\*)To find the critical path of the circuit, first switch the view mode from RTL view to technology view. To do this, press the and-gate symbol on the toolbar. After you press the and-gate, you are in technology view. Press the alarm clock symbol on the toolbar to view the critical path. This is for Synplicity only. XST does not allow you to see the critical path.

### **Implementation:**

(\*) Implementation takes the netlist file generated from synthesis and runs the implementation. This netlist file will be an .edf file for Synplify Pro or an .ngc file for XST. You do not need to change anything in implementation, single click on <implementation>. If you want to optimize later, you can look into the options.

(\*) Implementation shows up as a dialog wizard with implementation running. If you wish to terminate the implementation before it ends select <abort> at the bottom. Once implementation is done, click <close> at the bottom.

(\*) If you are using Synplicity, you may get a warning about timing not being met. This is okay. It means the synthesis tool thinks the design can run at X MHz, but the implementation tools realizes it will actually run slower than X.

(\*)To view the implementation reports select <reports> below implementation box.

### **Timing Simulation (i.e. post place-and-route simulation):**

(\*) Select <options> below timing simulation box. Under <general>,<input files> by default you will have a .sdf file generated from implementation and a TIME\_SIM.vhd file as the final netlist VHDL file. The .sdf gives the timing information for each gate and

wire in the circuit. Add your testbench to your input files. Again, this testbench should not have generic mappings to the entity under test.

(\*) Select top level unit as <Testbench>

(\*) Single click on <timing simulation>. Observe the waveform and save it. The waveform should now have propagation delay timing information.

### **Static Timing Analyzer:**

(\*) Go to <analysis> and single click on <static timing analyzer> will give you the timing report.

## **Option 2: Xilinx Environment (School)**

VHDL Simulator: Modelsim Special Edition (SE 6.3a)

Synthesis: Synplicity Synplify Pro (8.6.2) or Xilinx ISE Foundation XST (ISE 9.1 SP3)

Implementation: Xilinx ISE Foundation (ISE 9.1 SP3)

### **Synthesis:**

(\*) Add design files, make sure you initialize the environment to point to correct tools.

(\*) To the left hand corner under look under <Sources>, <Sources for> , <workspace name>, <device name> select your top-level source code file and then select <Synthesis/Implementation> under <Sources>, <Sources for>.

(\*)Then look under processes for <Synthesize>. Double-click on Synthesize to run synthesis.

(\*) Note that when you right click on <Synthesize> you can see several options; selecting them or double clicking on them will do the task specified.

### **RTL mode:**

(\*) Under Synthesize, you will also see <Launch Tools>, and you can view RTL and technology schematics.

### **Implementation:**

(\*) When done with synthesis, double click on <Implement Design> to run the implementation phase.

(\*) Note that when you right click on <Implement Design> you can see several options; selecting them or double clicking on them will do the task specified.

### **Post-translate simulation and Timing simulation (post-route simulation):**

(\*) You can also do post-translate simulation and post-route simulation by selecting them by looking under <Sources>, <Sources For>. Click until you get to your testbench file, when you should then see the ModelSim Simulator appear in the Processes window.

Post-translate simulation is roughly equivalent to Aldec's post synthesis simulation, in that there is no propagation delay timing information. Post-route simulation (which is the same as post place-and-route simulation) has propagation delay timing information because it is based on an .sdf file.

(\*) When you do post translate simulation and post route simulation, you may have to modify your testbench file to comment out references to generic mapping. Comment out generic ports in the component declaration and generic port maps in the component instantiation. After synthesis the top-level entity will not have generic ports any longer.

(\*) You can see the <Project Status>, <Device utilization summary> and <Detailed Reports> on the right side under the <Design Summary> window.

### **Static Timing Analyzer:**

(\*) When in the <Sources For> <Synthesis/Implementation> mode, you can look at the static timing analysis by selected <Generate Post Place and route Timing>, <Analyze Post Place and Route Timing>.