

Hands-On Session 1—VHDL Simulators

Option 1: Aldec Environment (School)

VHDL Simulator: Aldec Active-HDL (7.2 SP2)

Synthesis: Synplicity Synplify Pro (8.6.2)

Implementation: Xilinx ISE Foundation (ISE 9.1 SP3)

Get Started :

1. Create a new workspace.
2. Select the location to store your files and give a name to workspace. (There should NOT be any spaces in the path specified to store the files.)
3. Select option "Create an empty design with design flow".
4. Select/Check your flow settings as follows :
 1. For HDL Synthesis, push "Select" and choose Synplicity Synplify Pro 8.6 or Xilinx ISE/Webpack XST 9.1.
 2. For Implementation, push "Select" and choose Xilinx ISE/Webpack 9.1.
 3. For Family, choose "Xilinx 9x Spartan3."
5. Select your design name.
6. Add new file or save your files in "src" folder and click on :
Design -> add files to design...

Compile and Simulate :

1. Click on :
Design -> Compile all... (or press F11)
2. Open a New waveform.
3. Select testbench as top level in the Design Browser drop down menu (top left corner).
4. Select and add required signals in the waveform.
5. Press F5 or "Run For" for the specified time.

Option 2: Xilinx Environment (School)

VHDL Simulator: Modelsim Special Edition (SE 6.3a)

Synthesis: Synplicity Synplify Pro (8.6.2) or Xilinx ISE Foundation XST (ISE 9.1 SP3)

Implementation: Xilinx ISE Foundation (ISE 9.1 SP3)

Get Started :

1. Click on :
File -> New Project
2. Give a name to the project and select the location you want to store the project files. (There should NOT be any spaces in the path specified to store the files.)

3. Check/Select the device properties as follows :

Family : Spartan3

Device : XC3S50

Package : PQ208

Speed : -5

Synthesis Tool : “Synplify Pro (VHDL/Verilog)” or “XST (VHDL/Verilog) “

Simulator : Modelsim-SE VHDL

Preferred Language : VHDL.

4. Keep on clicking the next button till Finish.
5. Click on “New Source” or
Project -> add source... or add copy of source...

Compile and Simulate :

1. In sources box (left top), select Synthesis/Implementation from drop down menu, select your main code file, expand the synthesis tab from the processes box and click on “check syntax”.
2. In sources box (left top), select Behavioral Simulation from drop down menu, select your testbench file, expand the modelsim simulator tab from the processes box and click on “simulate behavioral model”.
3. Click on “Run” button after specifying time in the box.