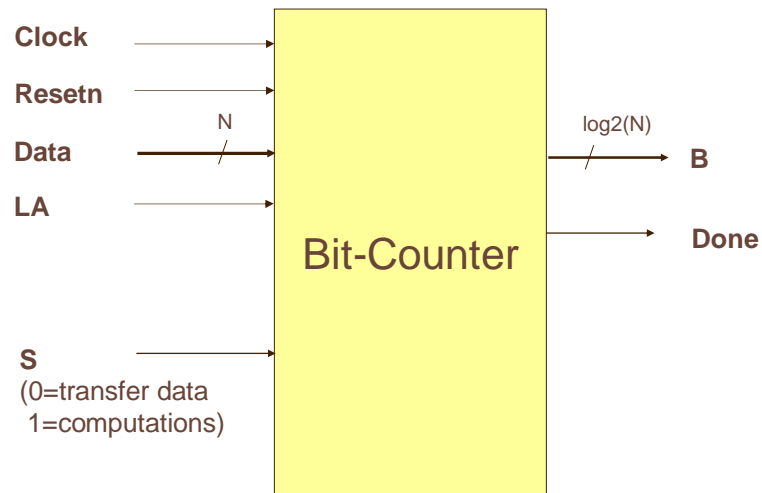


# ECE 545—Digital System Design with VHDL

## Bit-Counter ASM Example

## Bit-Counting – Required Interface



Specification: Count the number of 1's in Data

## Explanation of ports

- Inputs
  - **Clock**: the circuit clock
  - **Resetrn**: asynchronous circuit reset (active-low)
  - **Data**: N-bit input
  - **LA**: 1= load data at next rising clock edge, 0 = do not load data
  - **S**: system mode
    - 0 = write data initially or read results
    - 1 = do computations
- Outputs
  - **B**:  $\log_2(N)$ -bit output.
  - **Done**: Indicates the operation is done.

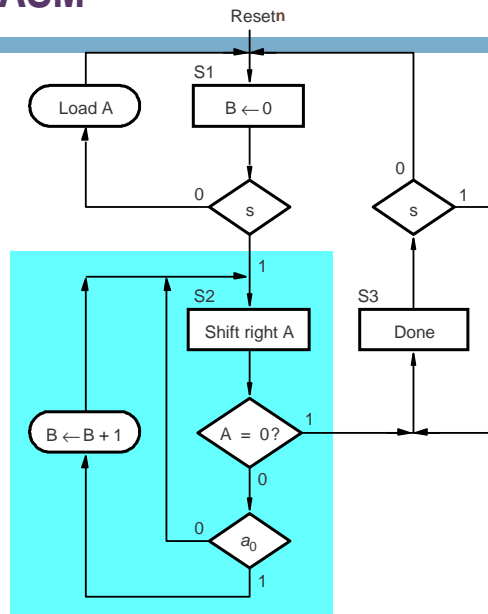
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## Step 1: Pseudocode

```
[load data into A]
B = 0 ;
while A ≠ 0 do
    if  $a_0 = 1$  then
        B = B + 1 ;
    End if;
    Right-shift A ;
End while;
[send done flag]
```

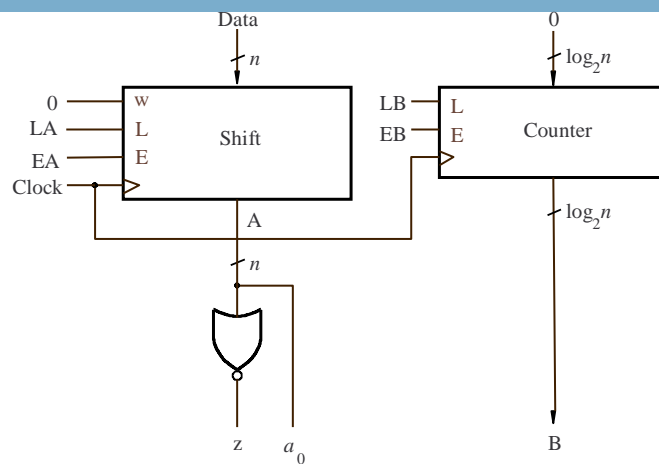
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## Step 2: High-Level ASM



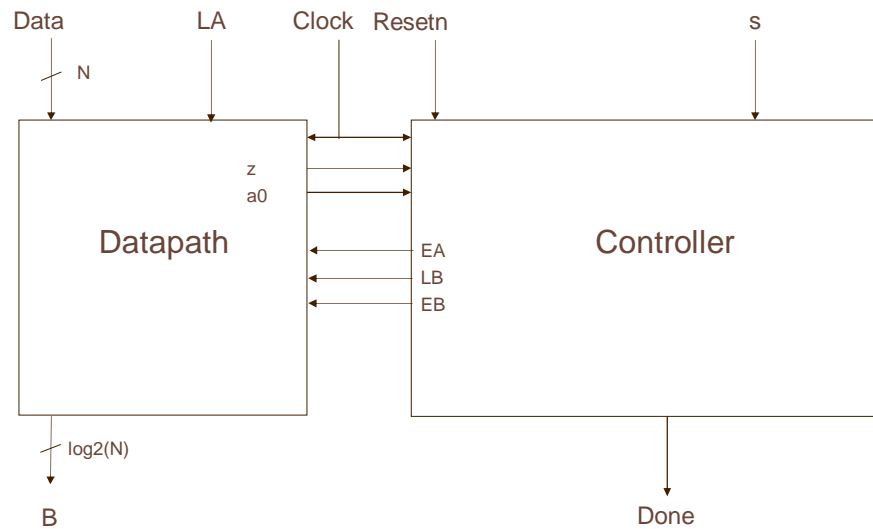
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## Step 3: Datapath Block Diagram



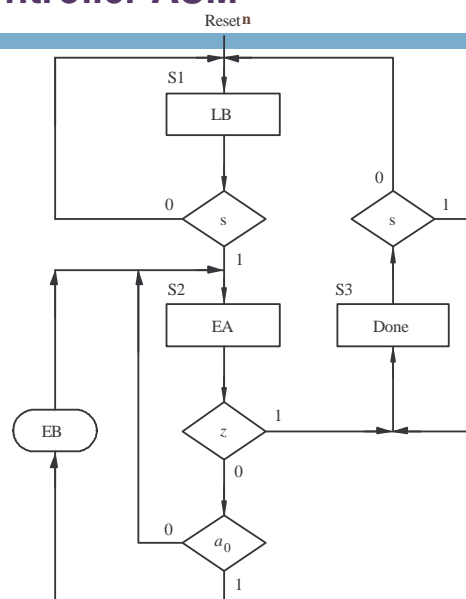
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## Step 4: Top-Level Interface Diagram



7

## Step 5: Detailed Controller ASM



8

# Waveform

