Proposed Working Draft

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Information Technology - AT Attachment Packet Interface (ATAPI)

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ABSTRACT

The standard for AT Attachment Interface with Extensions (ATA-2) has been completed, but as the popularity of the interface has increased, its application area has grown outside the originally intended purpose. This draft proposed standard is based upon the AT Attachment Interface with Extensions (ATA-3). This document is a stand alone document, separate from that document. The AT Attachment Packet Interface (ATAPI) standard is intended to broaden the ATA scope and application area and take advantage of the huge installed BIOS (Basic Input/Output System) base, and software.

This standard defines a SCSI Like packet interface protocol for use with the ATA protocol defined in ATA-3.

The ATAPI standard shall maintain a high degree of compatibility with the AT Attachment with Extensions (ATA-3) while providing documentation for additional capabilities. This standard is not intended to require changes to presently installed devices or existing software. It is intended that this standard would be used to provide additional capabilities.

The proposed ATAPI standard involves evolutionary expansion of the draft AT Attachment with Extensions standard to provide additional capabilities. The nature of the proposed project is to enable the attachment of devices other than disk drives to the physical AT Attachment interface as defined in the ATA-3 standard. This insures that current investments in AT Attachment are provided with more stability in the face of technological developments. It is likely that any isolated negative impacts would occur in any case through non-standard evolution or revolution.

PATENT STATEMENT

CAUTION: The developers of this standard have requested that holders of patents that may be required for the implementation of the standard, disclose such patents to the publisher. However, neither the developers nor the publisher have undertaken a patent search in order to identify which, if any, patents may apply to this standard.

As of the date of publication of this standard and following calls for the identification of patents that may be required for the implementation of the standard, no such claims have been made.

Change History

Rev 0.2 -> Rev 0.3, Aug 20, 1995

1. **Remove bottom 4 Bullet Items from Section 3.5.1**
2. **Remove section 3.5.2.1**
3. **Remove bottom 2 bullets from section 4.6**
4. **Change Bit 0 of Status registers from ERROR to CHECK.**
5. **Move "BIOS & ATAPI Driver Compatibility" section to Annex A**
6. **Add "**ATAPI device should wait until SRST is cleared by the host before completing their SRST sequence." **to Annex A "6.2.1 SRST Initialization Sequence"**
7. **Change "Draft Standard" to "Standard"**
8. **Remove "Proposal"**
9. **Remove last Two Lines of last paragraph of ABSTRACT.**
10. **Change 0xnn to 0nnh for Hex.**
11. **Remove DASP & PDIAG sequence from SRST in "ATAPI Implementation of ATA SRST".**

Rev 0.3 -> Rev 1, Sep 19, 1995

1. **Global search and replacement of Will, May and Could.**
2. **Global search and replacement of SERVICE with DSC.**
3. **Global search and replacement of CoD with C/D-.**
4. **Global search and replacement of EXECUTE DIAGNOSTICS with EXECUTE DRIVE DIAGNOSTICS.**
5. **Capitalize Commands.**
6. **Replace section 2.2 Signal Conventions with ATA-3 text.**
7. **Move Abbreviations to their own section.**
8. **Move section 3.5.2 Redundant Command Functionality to Informative Annex.**
9. **Clean up DRQ & BSY sequencing.**
10. **Delete 2nd paragraph of section 4.10.1 Release.**
11. **Move Note to bottom of figure 4.**
12. **Remove item 11 from section 4.11.**
13. **Add SERVICE to header in section 5.7.**
14. **Change note 1 in table 9 from superscript to "(1)" and make note part of table graphics.**
15. **Remove note from description of bit 4 in table 10.**
16. **Change Sense Key to ATAPI Sense Key in table 11.**
17. **See change bars and revision 0.3 for additional changes.**

Rev 1 -> Rev 2, Oct 10, 1995

1. Add Embedded Graphics files
2. Global Search and replace of Task File with Command Block
3. Global search and replace of May, Will, Could, New, Old, Previous
4. Add ATAPI IDENTIFY DEVICE command description
5. Add descriptions for SET FEATURES commands required by overlap.
6. Clarification of Overlap protocol descriptions.
7. Clarification of Overlap protocol state diagrams.
8. Various editorial changes (shown in BOLD)

Table of Contents

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1. Scope

This document is intended to be used with the ATA-3 document. Its purpose is to describe the operation of the ATA Packet Interface Transport Mechanism (ATAPI-TM) and ATA Packet Interface Transport Protocol (ATAPI-TP). It indicates areas within the ATA document which are modified for operation of Packet Interface Protocols n the ATA environment. Both mandatory and optional specifications are presented.

In the event of a conflict between the ATA-3 document and this document, the interpretation of this document shall prevail only if this document acknowledges that a conflict exists between the documents.

This document provides a description for the ATAPI Transport Protocol (ATAPI-TP) and ATAPI Transport Mechanism (ATAPI-TM). Command sets for specific devices such as CD-ROM and Tape are defined in separate documents referencing this standard.

2. Conventions

2.1 Document Conventions

Certain words and terms used in this document have specific meaning beyond the normal English meaning. These words and terms are defined either in this section or in the text where they first appear. Names of signals, commands, statuses, and sense keys are in all uppercase (e.g. ATAPI IDENTIFY DEVICE). Lower case is used for words having the normal English meaning.

Fields containing only one bit are usually referred to as the <name> bit instead of the <name> field. Numbers that are not immediately followed by a lower case b or h are decimal (nnh for Hexadecimal, where nn refers to two hexadecimal digits 0-9, A-F.)

2.2 Signal Conventions

Signal names are shown in all upper case letters.

All signals are either high active or low active signals. A dash character (-) at the end of a signal name indicates it is a low active signal. A low active signal is true when it is below V_{iL}, and is false when it is above V_{iH}. No dash at the end of a signal name indicates it is a high active signal. A high active signal is true when it is above V_{iH}, and is false when it is below V_{iL}.

Asserted means that the signal is driven by an active circuit to its true state.

Negated means that the signal is driven by an active circuit to its false state.

Released means that the signal is not actively driven to any state. Some signals have bias circuitry that pull the signal to either a true state or false state when no signal driver is actively asserting or negating the signal. These cases are noted under the description of the signal, and their released state is stated.

2.3 Definitions

2.3.1 Command Packet (CP)

“Command Packet” is the structure used to communicate commands from a host computer to an ATAPI device.

2.3.2 Data Block

This term describes a data transfer, and is typically a single sector, except when declared otherwise by use of the Set Multiple command.

2.3.3 DMA (Direct Memory Access)

DMA is a means of data transfer between Device and host memory without processor intervention.

2.3.4 Field

A field is a group of one or more contiguous bits.

2.3.5 Ignore

Information in this field or bit shall not be used by the receiving device.

2.3.6 Invalid

Invalid refers to an illegal (reserved) or unsupported field or code value.

2.3.7 Logical Block

A Logical Block is a unit of data supplied or requested by a host computer.

2.3.8 Mandatory

“Mandatory” indicates that a referenced item is required to claim compliance with this standard.

2.3.9 One

“One” represents a true signal value or a true condition of a variable.

2.3.10 Optional

“Optional” describes features which are not required by the standard. However, if any feature defined by the standard is implemented, it shall be done in the same way as defined by the standard. Describing a feature as optional in the text is done to assist the reader. If there is a conflict between text and tables on a feature described as optional, the table shall be accepted as being correct.

2.3.11 Page

Several commands use regular parameter structures that are referred to as pages. These pages are identified with a value known as a page code.

2.3.12 Shall

Describes a mandatory requirement of the standard.

2.3.13 Should

Describes a recommendation within the standard..

2.3.14 Reserved

Reserved bits, fields, bytes, and code values are set aside for future standardization. Their use and interpretation may be specified by future extensions to this or other standards. A reserved bit, field, or byte shall be set to zero, or in accordance with a future extension to this standard. The recipient shall not check reserved fields.

2.3.15 Status

Status is one byte of information sent from the ATAPI device to the host computer upon completion of each command.

2.3.16 Vendor Specific - VS

The term, VS, is used to describe bits, bytes, fields, code values and features which are not described in this standard, and may be used in a way that varies amoung vendors.

2.3.17 Zero

Zero is a false signal value or a false condition of a variable.

2.4 Symbols and Abbreviations

2.4.1 ATA (AT Attachment)

ATA defines a compatible register set and a 40-pin connector and its associated signals.

2.4.2 AWG

American Wire Gauge

2.4.3 CHS (Cylinder-Head-Sector)

This is an ATA term defining the address translation of the drive as being by physical address. This form of addressing is not used by ATAPI Devices.

2.4.4 LBA (Logical Block Address)

The LBA defines the address translation of the drive by the linear mapping of sectors from 0 to n.

2.4.5 LSB

Least significant bit

2.4.6 LUN

Logical Unit Number.

2.4.7 MSB

Most significant bit

2.4.8 PIO (Programmed Input/Output)

PIO is a means of data transfer that requires the use of the host processor.

2.4.9 SAM

2.4.10 SCSI Architectural Model. X3T10/994D

3. ATAPI Overview

The purpose of the ATAPI is to provide a more extensible and general purpose interface than the ATA Command Block.

Although a device attached to the ATAPI Interface utilizes the ATA Host Hardware and Command Block, the logical interface differs slightly and needs to support additional capabilities. The Mass Storage devices connected to the ATA Bus make use of eight (Command Block) registers that contain the command and all parameters needed for operation. However, eight registers is not enough to pass all the needed information for commanding other Device types. To remedy this, the ATAPI Device receives its commands through the use of an ATAPI PACKET command, in addition to the normal ATA protocol. The ATAPI PACKET command complements the existing ATA commands. The ATAPI Device shall support all of the ATA specified protocol, including the Reset Master/Slave Diagnostic Sequence, Diagnostic Command, and Command Abort for unsupported Commands. The ATAPI Device shall also support both the Master and Slave modes of operation.

3.1 ATA Signal Utilization

ATAPI Devices utilize the signals and timing definition from the ATA-3 Standard.

3.2 ATA Command Utilization

The ATA Command Block concept does not contain enough bytes to support some of the command structures of non-disk Devices, so a _ command called “Packet Command” has been added to allow a Packet to be sent to the Device. The Packet data is transferred by writing multiple times to the Data Register. No random access to the Command Packet in the Device is possible. This technique reduces the number of register addresses needed, but not the actual space needed. Although all the commands for the ATAPI Device could be sent via this packet protocol, some of the existing ATA commands and the full ATA command protocol are necissary for the existing drivers to operate correctly. The ATAPI Devices therefore support some existing ATA commands in addition to the ATAPI PACKET command, so that there are be minimal changes to the drivers. This minimal set of ATA commands is different than the minimum as defined in the ATA standard, but should be sufficient for normal operation.

3.3 ATA Compatibility

There are several backward compatibility issues with the ATA commands, and therefore the ATAPI Devices respond to the existing ATA Reset Master/Slave Diagnostic Sequence, but not the ATA Identify Drive or ATA Read commands. This allows ATAPI device to work with BIOS and ATA drives developed before this standard was available. All unsupported ATA commands shall be Aborted, and not executed. As with aborted commands in ATA, an interrupt is generated to signal the completion with an “aborted” error status.

3.4 Packet Types

To allow for generic packet transfer and the connection of SCSI like Devices, there shall exist a minimum set of information that is exchanged. This information shall generically support the following:

- Command Packet (Always padded to number of bytes identified in byte 0 of the identify drive data. 00 = 12 bytes, 01 = 16 bytes)
- Command Parameter Data (e.g. Write Data etc.)
- Command Response Data (e.g. Read Data etc.)
- Status. The Status will be presented using the ATAPI Status Register (redefinition of the ATA Status Register).
- ATAPI devices shall abort ATA commands not supported by the device.

1

4. ATAPI Protocol

ATAPI Devices are commanded by two methods, the original ATA Commands utilizing the traditional ATA Command Block and the PACKET COMMAND method. For both methods, the devices using this interface shall be programmed by the host computer to perform commands and return status to the host at command completion. The ATAPI protocol conforms to the ATA protocol except where specificlly modified by this standard.

The "Protocol" for ATAPI centers around the usage of an ATA Command called "PACKET COMMAND." All the normal ATA rules and protocol are used to issue the PACKET COMMAND, but once the command has been issued, a set of rules specific to ATAI PACKET COMMANDS applies:

1. The interpretation of the DRQ bit in the Status Register shall be used along with the Interrupt Reason Registers to determine the actual Interrupt Type.
2. The actual command for the Device to execute is sent as a packet via the data register, and not the Command Block.
3. Command arguments are supplied by the Command Packet as well as from the Command Block.
4. A Byte Count is used to determine the amount of data the Host shall transfer at each DRQ Interrupt.
5. The ATAPI Features Register is used to indicate when DMA is used rather than by using different opcodes.
6. The final status is presented to the Host as aninterrupt after the last data has been transferred, rather than along with the last block of data.

These rules (protocol) only apply from after the issuance of the PACKET COMMAND, until the Completion Status has been read by the Host. After the Completion Status has been read, the Command Block Register definitions and Protocol revert to the standard ATA definition.

4.1 Initialization

The ATAPI Device responds just as defined in the ATA Standard. The DASP and PDIAG signals are utilized following any reset condition, except the ATAPI RESET command.

4.2 PACKET COMMAND

The PACKET COMMAND is issued exactly as normal ATA commands, by initializing the Command Block Registers, setting the Drive Selection Bit and writing the Command byte into the Command Register. With normal ATA commands a DRQ (Optional Interrupt) would be generated to indicate that the data for the command could be transferred to/from the Device. With the PACKET COMMAND, the first DRQ indicates that the Command Packet Data shall be written to the Device. The Command Packet bytes shall always be transferred via PIO and never using DMA.

ATA PACKET COMMANDs may be issued regardless of the state of the DRDY Status Bit.

If while polling BSY the device remains in a state where it cannot accept a command for more than 5 seconds, the Host may time out and reset the device.

4.3 Status Register Utilization for PACKET COMMANDs

D7	D6	D5	D4	D3	D2	D1	D0	
BSY	DRDY	DMA READY	SERVICE	DRQ	CORR	Reserved	CHECK	Read

4.4 Byte Count Register (Cylinder Low/High) Usage for Packet Commands

D7	D6	D5	D4	D3	D2	D1	D0	
Byte Count (Bits 0-7)								R/W
Byte Count (Bits 8-15)								R/W

This register is used to control the number of bytes the Host shall transfer at each DRQ. It is only used for the command parameter data being transferred via PIO and never for DMA or Command Packet bytes.

Since the length of data that is actually transferred to and from an ATAPI Device using PIO is controlled by the Host, and since the ATAPI Device needs to be able to control the number of bytes transferred, an additional capability was needed. By using the Byte Count Register, a capability to transfer a variable number of bytes has been created. In ATAPI the Device indicates to the Host the number of bytes that shall be transferred on each DRQ Interrupt. Before transferring data, the Host shall read the 16-bit Byte Count Register, and comply with the length requested. Both the ATAPI Device and the Host have their own byte counts and transfer until those counts go to zero. For some commands, such as Mode Sense, the Host does not know the amount of data that be transferred, and shall rely on the Byte Count supplied by the Device to transfer the correct amount of data.

A further capability of the Byte Count Register is for the Host to signal to the ATAPI Device the maximum amount of data it may take in a single PIO DRQ or DMA DMARQ packet and/or the preferred packet size. For all commands that require data be transferred to the host, the Host shall set the Byte Count Register to the desired length before issuing the PACKET COMMAND. This length shall be used by the ATAPI Device as the maximum size for each PIO or DMA data packet. The Device may choose to transfer packets smaller than those set by the host in the Byte Count Register.

For all commands that transfer all the data in one DRQ Interrupt, the Byte Count shall contain the total data length. When a Read command is being processed, the ATAPI Device may wish to send all the data that is available in its buffers on just one DRQ Interrupt, with the limitation that only 65535 bytes may be transferred at one time.

Table 2 - Byte Count Register Usage

Operation	Usage (PIO)	Usage (Non-Overlapped DMA)
Send Command Packet	Is used as a parameter to the PACKET COMMAND and is not used to control the Packet transfer.	Command Packet is always sent via Programmed I/O and not DMA.
Parameters to the PACKET COMMAND (Command Block Contents)	As a parameter to any PACKET COMMAND that transfer parameter data, the Byte Count is used by the Host to communicate the maximum / preferred amount of data to be transferred on each DRQ.	The Device may ignore the byte count, as the actual transfers are controlled via the ATAPI Device and not the Host.
Parameter Data from the Device to the Host (e.g. data from a Read, or Inquiry command)	At each DRQ the count contains the number of bytes that the Host shall transfer from the Device.	The ATAPI Device may request data transfer whenever it wishes, and as such the Byte Count shall not be used.
Parameter Data from the Host to the Device (e.g. data for a Write, or Mode Select command)	At each DRQ the count contains the number of bytes that the Host shall transfer to the Device.	The ATAPI Device may transfer data whenever it wishes, and as such the Byte Count shall not be used.

If the Device requests more data be transferred than required by the command protocol, the Host shall pad when sending data to the Device.

The only permissible time for an actual Odd Byte Count value is on the Last DRQ. Intermediate DRQs shall contain even byte counts.

The Device is not responsible for padding the data. Only the specific amount of data specified by the host byte count shall be transferred.

4.5 Sector Count (ATAPI Interrupt Reason) Register Usage for PACKET COMMANDs

D7	D6	D5	D4	D3	D2	D1	D0	
Reserved					RELEASE	IO	C/D-	Read

The Interrupt Reason Register contains an expanded definition of the ATA DRQ Status. When the DRQ is presented in the ATAPI Status Register for an ATAPI PACKET COMMAND, then the contents of this register indicate if PACKET COMMAND or Parameter data shall be transferred and, if so, the direction of the transfer.

4.6 Immediate Command Operation

Immediate ATAPI PACKET COMMANDs return Completion Status immediately, with the actual execution of the command continuing. When the actual completion of the seek operation of immediate ATAPI PACKET COMMANDs has occurred, the Device shall set the SERVICE bit in the Status Register.

- Immediate ATAPI PACKET COMMANDs that report completion before the actual completion (e.g., CD-ROM Seek, Play Audio, etc.) shall respond by queuing the command.
- New ATAPI PACKET COMMANDs received while a Prior PACKET COMMAND is still executing shall cause both commands to be aborted with an error, “Check Condition”.
- If an Immediate ATAPI PACKET COMMAND is executing when the device is issued an SRST the SERVICE bit shall not be cleared with the rest of the status register. Instead the functionality of the SERVICE bit shall be maintained.

ATAPI immediate commands use the ATAPI SERVICE bit to inform the host that an overlapped operation has completed using the same protocol as the ATA seek command using the ATA DSC bit.

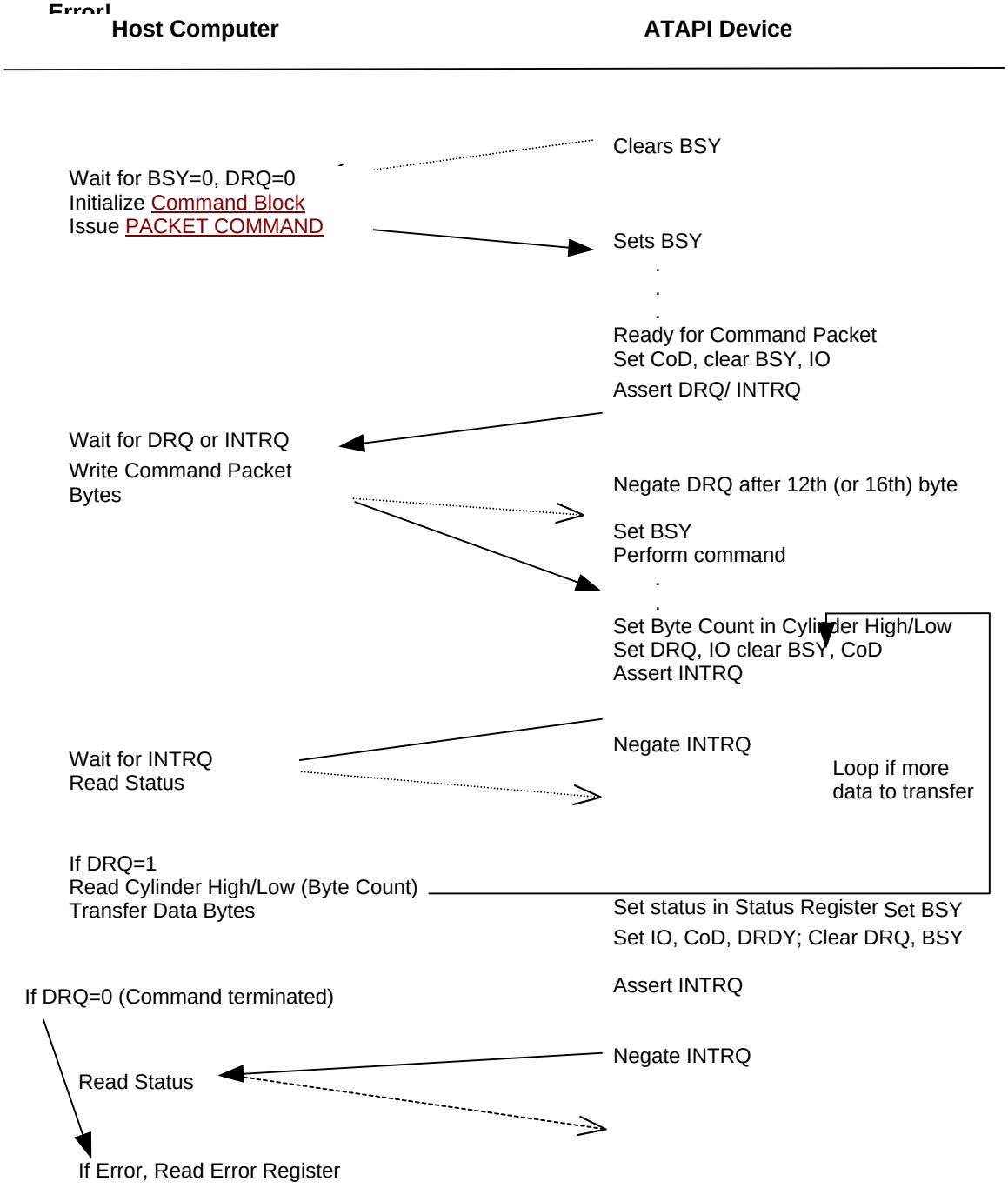
4.7 Flow of Non-Overlapped PACKET COMMAND, PIO Data In to Host

This class of PACKET COMMANDs includes commands such as Inquiry, Read etc. Execution includes the transfer of some number of data bytes from the Device to the host.

1. The host Polls for BSY=0, DRQ=0 then initializes the Command Block by writing the required parameters to the Features, Byte Count, and Drive/Head registers.
2. The host writes the PACKET COMMAND code (A0h) to the Command Register.
3. The Device sets BSY, before the next Host read of the status register, and prepares for Command Packet transfer.
4. When the Device is ready to accept the Command Packet, the Device sets C/D- and clears IO, BSY prior to asserting DRQ. Some Devices assert INTRQ following the assertion of DRQ.
5. After detecting DRQ, the host writes the 12 or 16 bytes of Command to the Data Register.
6. The Device(1) clears DRQ (when the last byte is written), (2) sets BSY, (3) reads Features and Byte Count requested by the host , (4) prepares for data transfer.
7. When data is available, the Device:(1) places the byte count of the data available into the Cylinder High and Low Registers, (2) sets IO and clears C/D-, (3) sets DRQ and clears BSY, (4) sets INTRQ.
8. After detecting INTRQ, the host reads the DRQ bit in the Status Register to determine how it shall proceed with the command. If DRQ= 0 then the device has terminated the command. If DRQ=1 then the host shall read the data (number of bytes specified in the Cylinder High/Low Registers) via the Data Register. In response to the Status Register being read, the Device negates INTRQ for both cases.
9. The Device clears DRQ. If transfer of more data is required, the Device sets BSY before clearing DRQ and the above sequence is repeated from step 7.
10. When the Device is ready to present the status, the Device places the completion status into the Status Register, sets C/D-, IO, DRDY, DRQ and clears BSY, prior to asserting INTRQ.
11. After detecting INTRQ, DRQ cleared and BSY cleared, the host reads the Status Register and if necessary, the Error Register for the command completion status.

The DRQ signal is used by the device to indicate when it is ready to transfer data, and is cleared after (during) the last byte of data to be transferred. This applies for both Command Packet as well as normal read/write data.

Error!



Solid Lines indicate control flow, and dotted lines are actions taken but without direct control flow change occurring. This Diagram is for Visualization only, design to text.

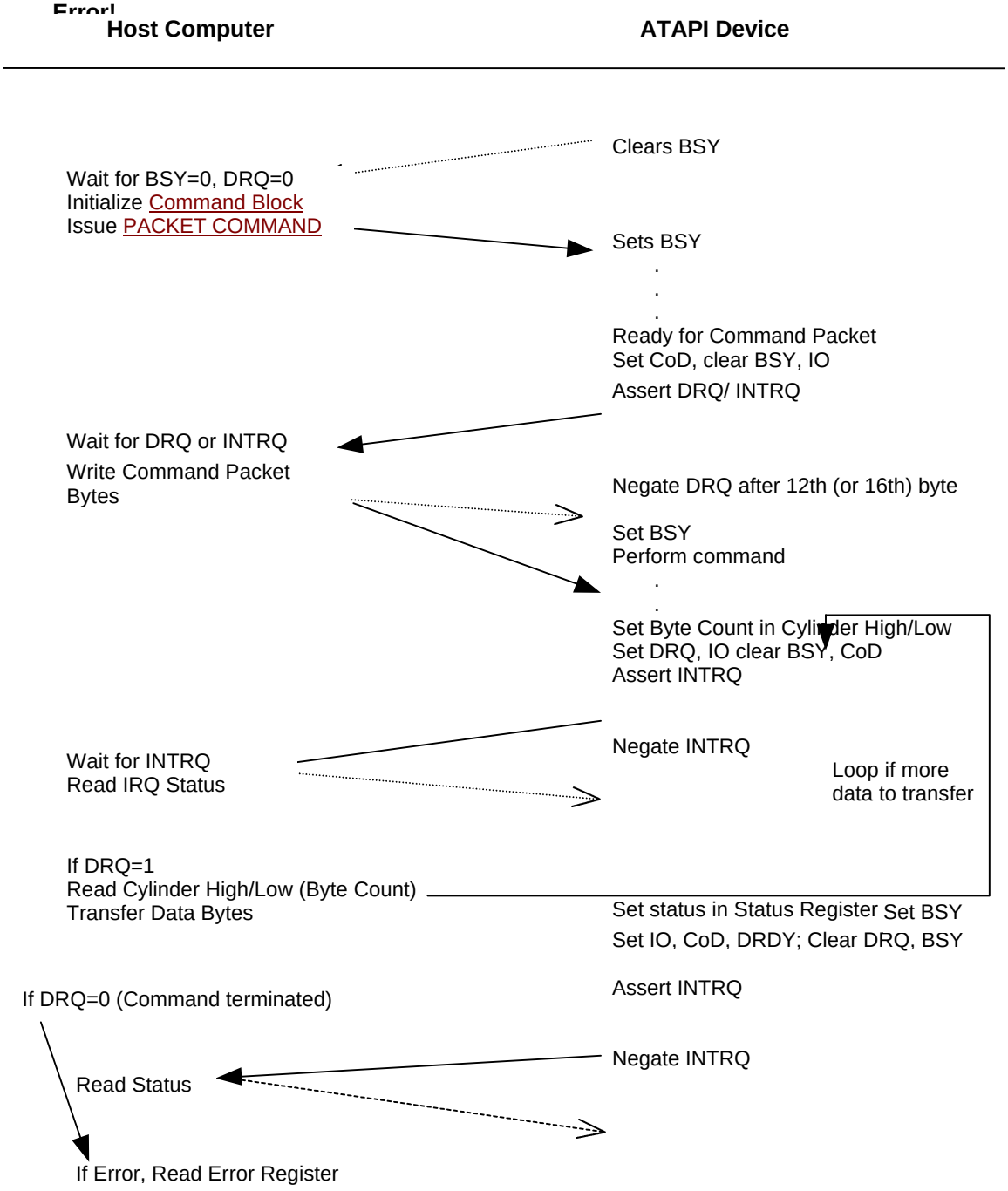
Figure 1 - Packet Comand with PIO Data In to Host

4.8 Flow of Non-Overlapped PACKET COMMAND with PIO Data Out from Host

This class includes commands such as Mode Select, Write etc. Execution includes the transfer of some known number of data bytes from the Host to the Device.

1. The host Polls for BSY=0, DRQ=0 then initializes the Command Block by writing the required parameters to the Features, Byte Count, and Drive/Head registers.
2. The host writes the PACKET COMMAND code (A0h) to the Command Register.
3. The Device sets BSY, before the next Host read of the status register, and prepares for Command Packet transfer.
4. When the Device is ready to accept the Command Packet, the Device sets C/D- and clears IO, BSY prior to asserting DRQ. Some Devices assert INTRQ following the assertion of DRQ. DRQ may be set before or after BSY has been de-asserted; however, DRQ is not visible to the host until BSY=0.
5. After detecting DRQ, the host writes the 12 or 16 bytes of Command to the Data Register.
6. The Device(1) clears DRQ (when the 12th byte is written), (2) sets BSY, (3) reads Features and Byte Count requested by the host, (4) prepares for data transfer.
7. When ready to transfer data, the Device:(1) sets the byte count (Cylinder High and Low Registers) to the amount of data that the Device wishes to be sent, (2) clears IO and C/D-, (3) sets DRQ and clears BSY, (4) sets INTRQ. The Byte Count would normally be set to the number of bytes requested by the contents of the register at the receipt of the command, but may be any amount that the Device may accommodate in its buffers at this time.
8. After detecting INTRQ, the host reads the DRQ bit in the Status Register to determine how it shall proceed with the command. If DRQ= 0 then the device has terminated the command. If DRQ=1 then the host shall write the data (number of bytes specified in the Cylinder High/Low Registers) via the Data Register. In response to the Status Register being read, the Device negates INTRQ for both cases.
9. The Device clears DRQ. If transfer of more data is required, the Device sets BSY before clearing DRQ and the above sequence is repeated from step 7.
10. When the Device is ready to present the status, the Device places the completion status into the Status Register, sets C/D-, IO, DRDY, DRQ and clears BSY, prior to asserting INTRQ.
11. After detecting INTRQ, DRQ cleared and BSY cleared, the host reads the Status Register and if necessary, the Error Register for the command completion status.

The DRQ signal is used by the device to indicate when it is ready to transfer data, and is cleared after (during) the last byte of data to be transferred. This applies for both Command Packet as well as normal read/write data.



Solid Lines indicate control flow, and dotted lines are actions taken but without direct control flow change occurring. This Diagram is for Visualization only, design to text.

Figure 2 - PACKET COMMAND with PIO Data Out from Host

4.9 Flow of Non-Overlap DMA Data Commands

This class includes commands such as Read, Write etc. Execution includes the transfer of some number of data bytes. ATAPI DMA data commands transfer parameter data using DMA. Command packet bytes for all ATAPI commands are issued using the ATAPI PIO command packet protocol.

1. The host Polls for BSY=0, DRQ=0 then initializes the Command Block by writing the required parameters to the Features, Byte Count, and Drive/Head registers. The host also initializes the DMA engine which services the Devices requests.
2. The host writes the PACKET COMMAND code (A0h) to the Command Register.
3. The Device sets BSY and prepares for Command Packet transfer.
4. When the Device is ready to accept the Command Packet, the Device sets C/D- and clears IO, BSY prior to asserting DRQ. Some Devices assert INTRQ following the assertion of DRQ.
5. After detecting DRQ, the host writes the 12 or 16 bytes of Command to the Data Register.
6. The Device(1) clears DRQ (when the 12th byte is written), (2) sets BSY, (3) reads Features and Byte Count requested by the host, (4) prepares for data transfer.
7. When ready to transfer data, the Device transfers via DMARQ/DMACK any amount that the Device may accommodate or has in its buffers at this time. This continues until all the data has been transferred.
8. When the Device is ready to present the status, the Device places the completion status into the Status Register, sets C/D-, IO, DRDY, DRQ and clears BSY, prior to asserting INTRQ.
9. After detecting INTRQ, DRQ cleared and BSY cleared, the host reads the Status Register and if necessary, the Error Register for the command completion status.

4.10 Flow of Non-data Immediate Commands

This class includes commands such as Seek, etc. Execution of these commands involves no data transfer.

1. The host Polls for BSY=0, DRQ=0 then initializes the Command Block by writing the required parameters to the Features, Byte Count, and Drive/Head registers.
2. The host writes the PACKET COMMAND code (A0h) to the Command Register.
3. The Device sets BSY and prepares for Command Packet transfer.
4. When the Device is ready to accept the Command Packet, the Device sets C/D- and clears IO, BSY prior to asserting DRQ. Some Devices assert INTRQ following the assertion of DRQ.
5. After detecting DRQ, the host writes the 12 or 16 bytes of Command to the Data Register.
6. The Device sets BSY and executes the command.
7. Upon compleetion of the command, the Device places the completion status into the Status Register, and sets IO, C/D-, DRDY and clears BSY, DRQ, prior to asserting INTRQ.
8. After detecting INTRQ, the host reads the Status Resister for the command completion status.

4.11 Timing of Non-Overlap Packet Command

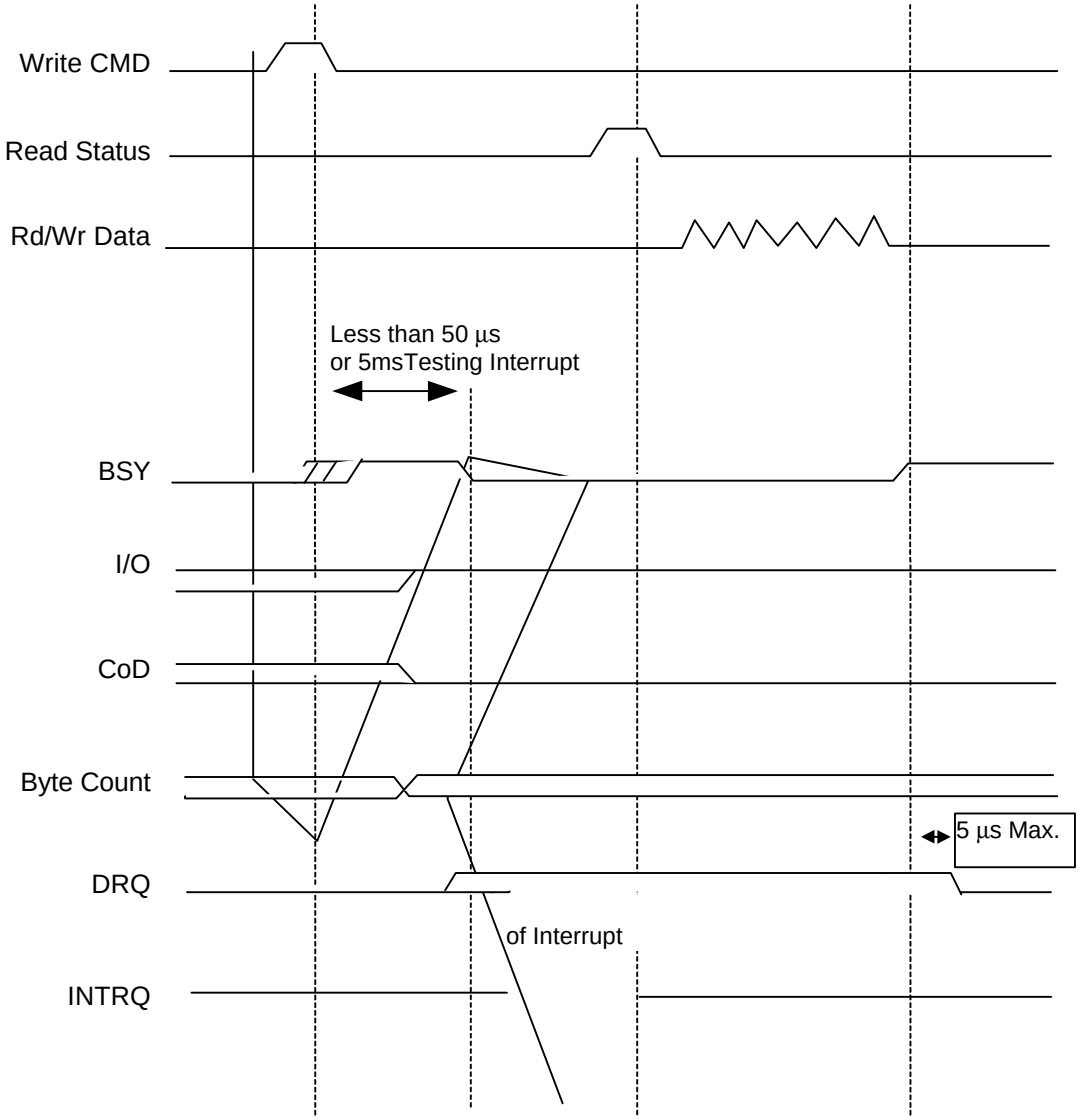


Figure 3 - Timing of Command Packet Transfer

4.12 Timing of Non-Overlap Data and Status Transfer

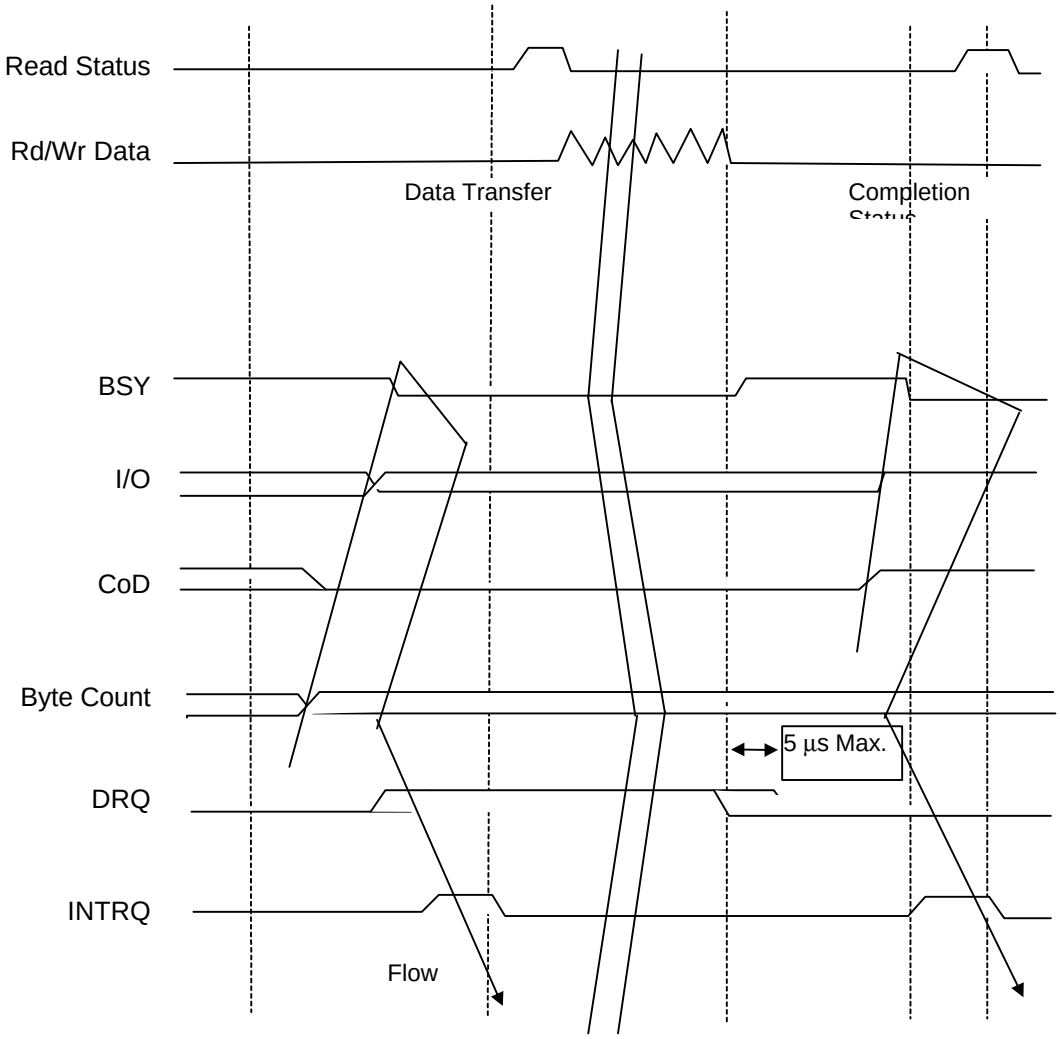
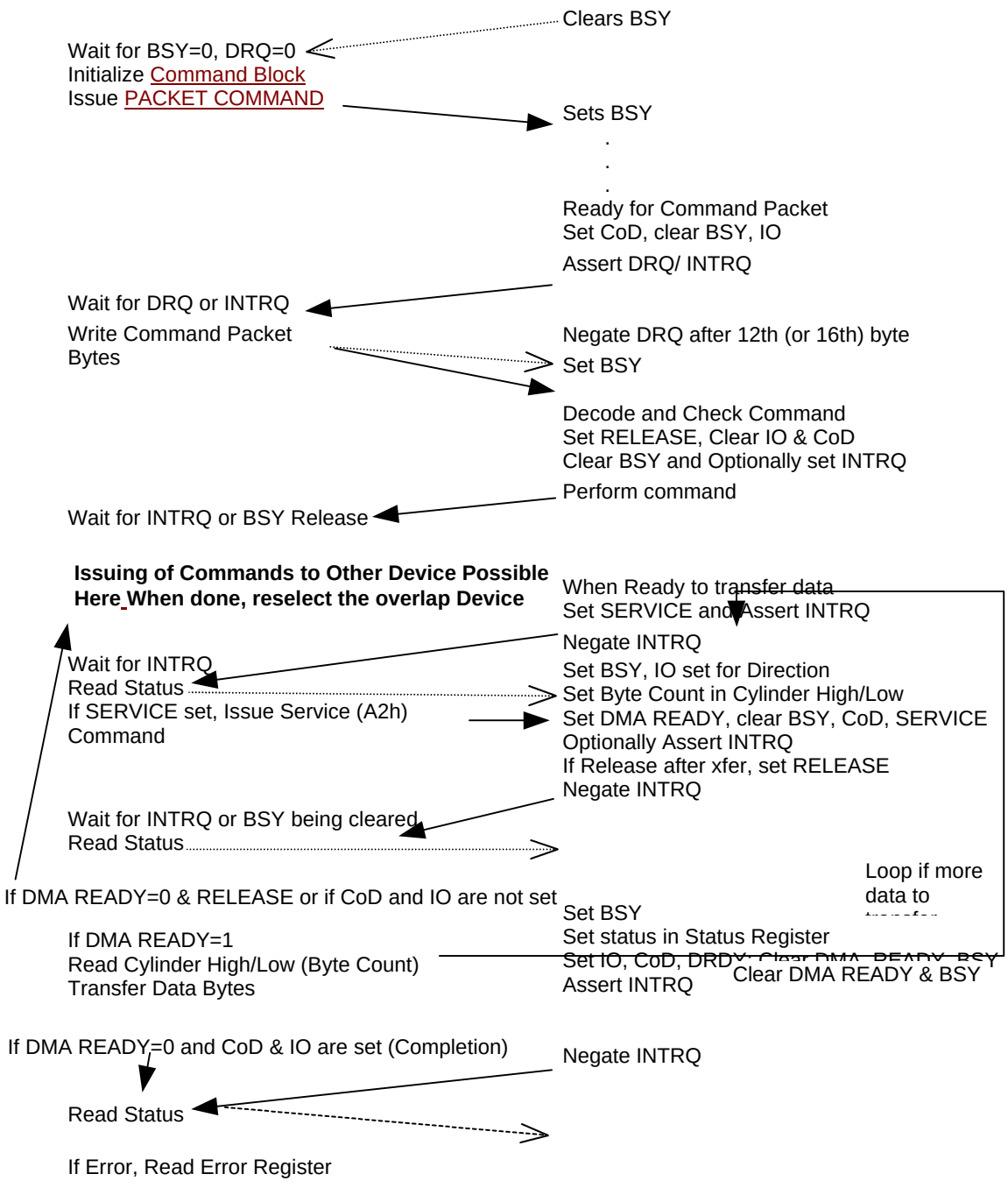


Figure 4 - Timing of Data and Status Transfer



Solid Lines indicate control flow, and dotted lines are actions taken but without direct control flow change occurring. This Diagram is for Visualization only, design to text.

Figure 5 - PACKET COMMAND with DMA Data

4.13 Overlapped Command Operation

ATAPI devices reporting support for Overlapped commands are capable of improving Host performance by releasing the Bus to another device before completing a command in progress. The host may enable this feature by setting the OVERLAP bit in the Feature Register when it issues an ATAPI PACKET COMMAND. The device uses the RELEASE bit in the ATAPI Interrupt Reason register to notify the host that it has released the Bus before it has completed the command in progress.

- Releasing the Bus to another device is at the discretion of the device processing an Overlapped command. Devices should only Release the Bus, before a command has completed, when the host does not need to service an Interrupt or DRQ from the device for more than the time specified in words 71 and 72 of the devices identify drive data. This is typically the case for seeks on mechanically slower devices such as CD-ROM and Tape.
- When the host detects a “Release” from a device to which it has sent an overlapped command, the DRV bit may be changed to select another device and issue a command.
- Changing the DRV bit while BSY or DRQ are set may cause the currently selected device to abort any command in progress.
- The normal protocol for Non-Overlapped commands requires that the command complete before the host may select another device. This means that the host is not able to access the Overlapped device again until the non overlapped device completes any command the host may issue to it.
- Fairness between slower Overlapped and faster Non-Overlapped devices sharing the same Bus, may be achieved by polling the slower Overlapped device’s SERVICE bit before issuing each command to the faster non-Overlapped device.
- When the host detects that the SERVICE bit in the ATAPI STATUS Register is set, a Service (A2h) command shall be issued before any Command Block registers besides ATAPI STATUS are valid.
- Once the Service (A2h) command has successfully completed the host may service the device’s interrupt as if the device were the only device on the Bus.
- Slower Overlapped devices may release control of the Bus several times while processing an overlapped command.
- When DMA data is to be transferred, the protocol sequence used for PIO is followed. When data is to be transferred a Service Interrupt shall be generated. No data shall be transferred until the Service (A2h) command has been received by the Device.
- The number of bytes that shall be transferred is specified in the BYTE COUNT Register after the Service (A2h) command has been processed. After the specified number of bytes is transferred the Bus shall either be released or held busy until data or status are available.
- At the completion of data transfer, if the Device shall “Release” the Bus, BSY shall be cleared in less than 5ms.

4.13.1 Release

One of the capabilities that is the foundation for Overlapped operation is Release. There are three different forms of release used in this specification, after the receipt of a Command, after transferring some data and after the receipt of the Service Command.

The device shall copy the information in the Command Block Registers before clearing BSY. Although holding the BSY longer in some cases would most likely be acceptable from a Host performance standpoint, forcing the driver to poll for varying lengths of time is not. This standard requires the device to report the typical length of time that the device holds BSY set while unloading and then Releasing the Command Block Registers. To minimize the host performance impact of devices which take ms to release, this standard defines an Interrupt on Release Capability.

The Interrupt on Release capability is enabled by the Host Driver using a SET FEATURES Command. To assist the Driver in determining if the Interrupt should be enabled the IDENTIFY DRIVE Command returns the length in microseconds that the device uses to Release for both an Overlapped Command and the Service Command. The Driver may then make its own decision to enable the interrupt. Thus if the Device reports 1000 ms, the Driver could decide that it wants to poll and not enable the interrupt.

The Release after Service Command shall only occur after the parameters for the Interrupt are loaded into the Command Block by the device. The time required by the device to perform the Release after the SELECTION Command shall be less than 5ms.

4.13.2 SERVICE (A2h)

Host arbitration of the Command Block Registers is performed by logic outside of the Devices attached to the ATA Bus. The SERVICE command is used by the host to return control of the command block registers to the device after the device has released control of the command block registers by releasing the ATA Bus to the Host.

When an overlapped command requests service the Host Driver shall determine which device needs to be serviced, and then issuing the Service Command. The service command allows the device to place information on the reason for the service into the Command Block registers.

Table 3 - Command Block Registers after the Service Command

Register	Contents
Data	
Error Register	If the Status indicates an Error then this is Valid
Reserved for ATA Tag	Reserved and not used by this Specification.
Interrupt Reason	Contains IO and C/D-
Tag for Command	Reserved for future use as Tag for the command requiring Service
ATAPI Byte Count LSB	Number of bytes that need to be transferred, both for PIO or for DMA
ATAPI Byte Count MSB	
Drive Select	Same before and after “Service”
Status	DRQ along with IO, C/D- and Release determine the reason for the Service Request
Floppy A Status	Unused
Floppy B Status	Unused
Unused	Unused
Floppy ID / Tape Control	Unused
Floppy Controller Status	Unused
Floppy Data Register	Unused
Alternate Status	Same as Status register
Change / Drive Address	Same before and after “Service”

4.13.3 Overlap Transitions

Table 4 - Overlap Transitions

State From	State To	Reason	Sequence	Notes
Idle	Cmd Packet	Host Issues A0h	BSY=1, C/D-=1, IO=0, DRQ=1, BSY=0	
Cmd Packet	Release	Command ok, but no data is ready to be transferred	BSY=1, DRQ=0, RELEASE=1, C/D-=0, IO=0, BSY=0, INTRQ=1 if Interrupt on Release After Command Packet is enabled	The time required by the Device to perform the Release is specified in Word 71 of the Identify Drive Data
Cmd Packet	Data Transfer	Command ok and Data is ready to be Sent/Received	BSY=1, DRQ=0, C/D-=0, IO=1/0, RELEASE=0, DRQ=1, BSY=0, INTRQ=1	The assertion of DRQ shall occur within the time specified in word 71 of the Identify Drive Data
Data Transfer	Release	# of bytes specified by the Byte Count Register has been transferred	RELEASE=1, DRQ=0 (BSY stays=0, C/D- & IO Stay the same)	The Release shall occur within 5ms after transferring the last word of data
Data Transfer	Data Transfer	# of bytes specified by the Byte Count Register has been transferred	BSY=1, DRQ=0, Byte Count =next count (C/D- & IO stay the same), DRQ=1, BSY=0, INTRQ=1	The assertion of DRQ shall occur within 5ms after transferring the last word of data from the Prior data transfer
Release	Service	Data or Status is ready for the Host	SERVICE=1, DMA READY=0/1, INTRQ=1	Requests that the Host Arbitrate and Issue the Service Command.
Service	Data Transfer	Service Command issued and Data may be transferred	BSY=1, IO=1/0, C/D-=0, Byte Count=x, DRQ or DMARQ=1 (DMA READY stays the same), BSY=0, INTRQ=1 if Interrupt on Service Comple-tion is enabled	
Service	Status	Service Command issued and Status is available	BSY=1, IO=1, C/D-=1, RELEASE=0, DRQ=0, BSY=0, INTRQ=1 if Interrupt on Service Completion is enabled	This is not a recommended transition. After transferring the data the device should set BSY until the status is available
Data Transfer	Status	# of bytes specified by the Byte Count Register has been transferred	BSY=1, RELEASE=0, DRQ or DMARQ=0, C/D-=1, IO=1, BSY=0, INTRQ=1	BSY shall be set within 5ms after transferring the last word of data if status is not available within the 5ms window

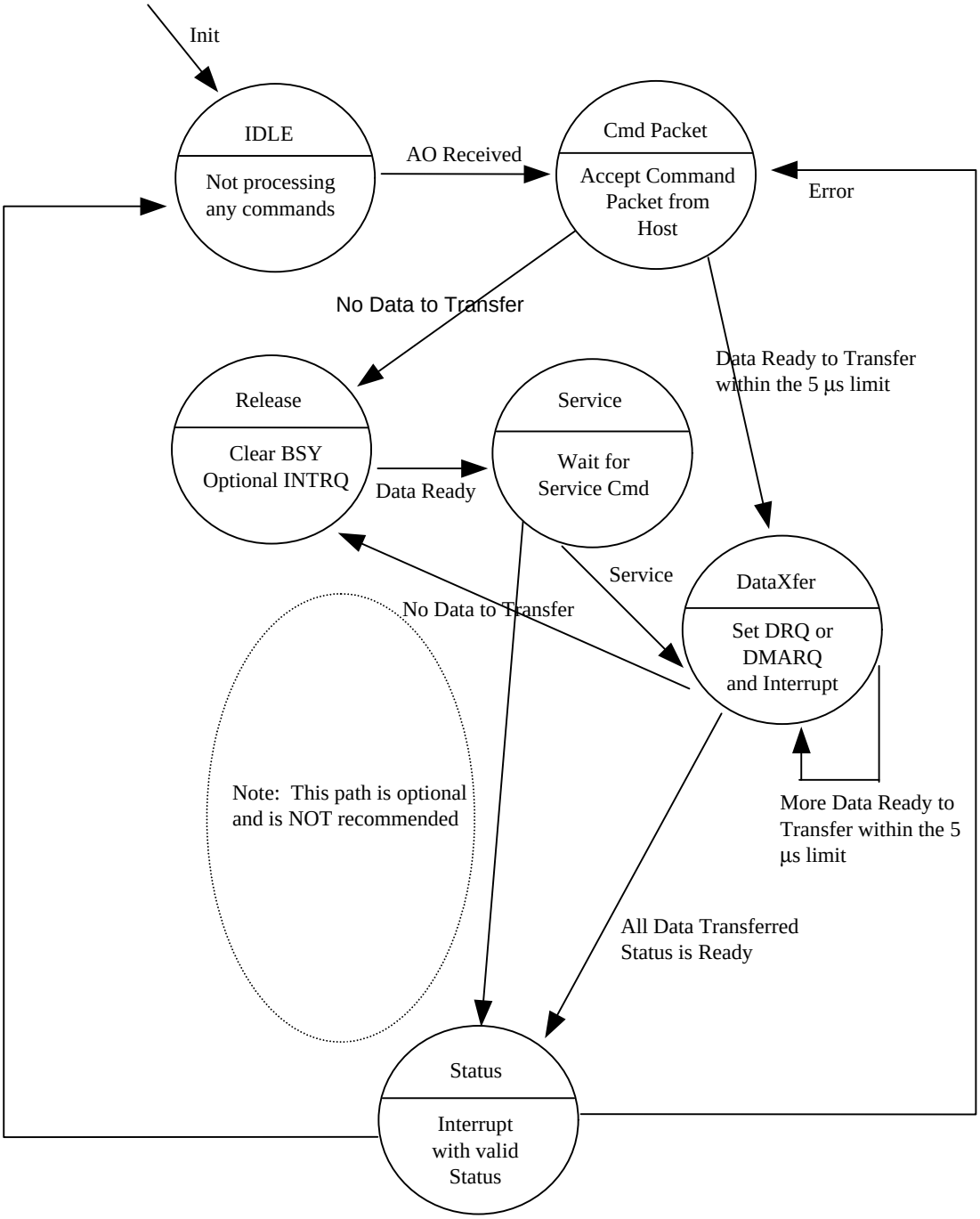
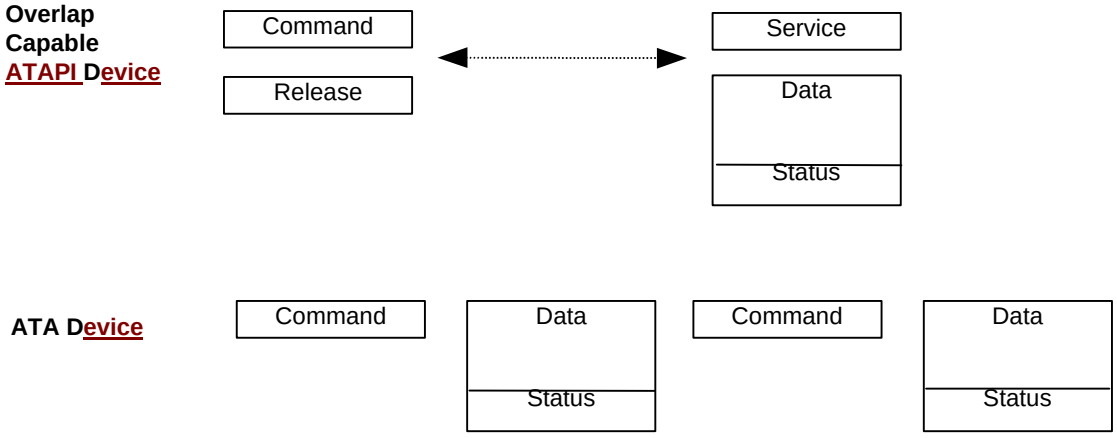


Figure 6 - State Diagram, Overlapped Operation, Legal Transactions

Note: Service to Status path is optional and NOT recomended.

4.13.4 ATAPI Overlap with only one ATAPI Device

- ATAPI Drive Releases the Command Block Ownership after acceptance of an ATAPI command.
- Overlap Mode is enabled on each command via the ATAPI Features Register.
- Overlapped Commands are issued to an ATA Drive while an ATAPI Command is still processing.
- Interrupts are generated from the selected device only. The Driver always selects the ATAPI Overlap capable device when there is no active command to an ATA Device.
- Device uses Interrupt & SERVICE Status to gain Host's attention. SERVICE Status set when any service is needed.
- Driver uses the A2h (Service) Command to give control of the Command Block Registers back to the Device after an Interrupt and Sensing the SERVICE status bit.
- The Interrupt Reason RELEASE Status bit is used to indicate a Release Interrupt.



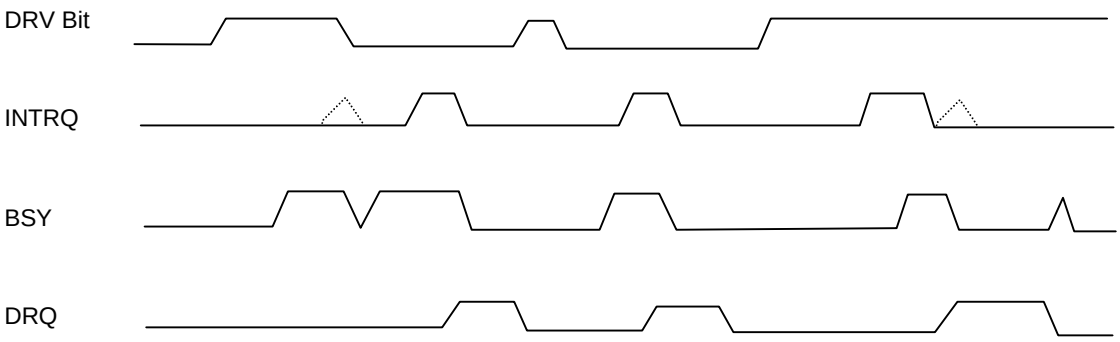


Figure 7 - ATAPI Overlap Command Sequence

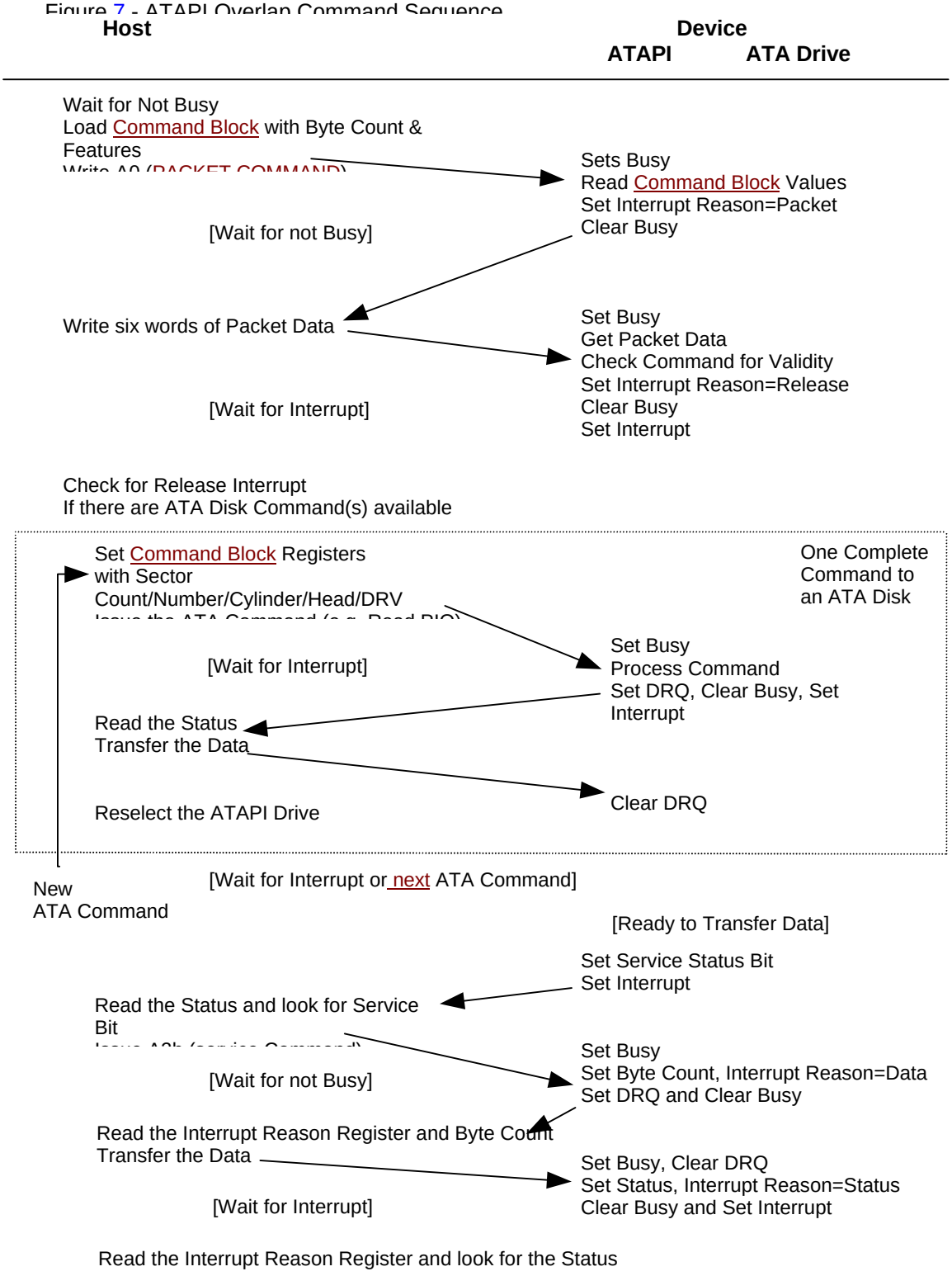


Figure 8 - ATAPI Overlap, One ATA Device and One ATAPI Device

4.13.5 Command Block ownership

When BSY or DRQ is set, the Command Block Registers are controlled by the Device, otherwise the Registers are controlled by the Host. When the device controlls the command block registers it may modify them and ignore any writes to them by the host. When the host controlls the command block the host may modify them and the device shall not.Table 55 - Registers Controlled by BSY & DRQ. 27

Logic conventions are: A = signal asserted, N = signal negated, x = does not matter which it is.
Bold are registers where ownership is controlled by BSY & DRQ.
Itallics are Registers that are not defined for use by ATA.

Per ATA protocol the host may abort any command by writing another command to the command register of the commnad block. The device shall abort the command in progress even though DRQ may have been set when the host wrote the new command.

Table 5 - Registers Controlled by BSY & DRQ

Addresses					Functions	
CS0	CS1	DA2	DA1	DA0	Read (DIOR-)	Write (DIOW-)
A	N	0	0	0	Data	
A	N	0	0	1	**Error Register**	**Features**
A	N	0	1	0	**ATAPI Interface Reason / Sector Count**	
A	N	0	1	1	**Sector Number**	
A	N	1	0	0	**ATAPI Byte Count LSB / Cylinder Low**	
A	N	1	0	1	**ATAPI Byte Count MSB / Cylinder High**	
A	N	1	1	0	**Drive Select**	
A	N	1	1	1	Status	**Command**
N	A	0	0	0	*Floppy A Status*	*Unused*
N	A	0	0	1	*Floppy B Status*	*Unused*
N	A	0	1	0	*Unused*	*Floppy Digital Output*
N	A	0	1	1	*Floppy ID / Tape Control*	*RESERVED*
N	A	1	0	0	*Floppy Controller Status*	*RESERVED*
N	A	1	0	1	*Floppy Data Register*	
N	A	1	1	0	Alternate Status	**Device Control**
N	A	1	1	1	**Change / Drive Address**	Unused

4.13.6 Error Handling with Overlapped Commands

Overlapped commands are enabled on a Command by Command basis. If an overlapped command is in progress and a non-overlapped command is then received, the Device aborts without status on any outstanding overlapped or queued command(s).

In overlapped operation there is intermediate command status, as well as the final command completion status. The intermediate status is supplied to indicate if the command was accepted. If the command is not accepted, then there is no further status supplied. The intermediate status is the status at the point that the device releases the Command Block registers back to the host, prior to executing the command. Thus this status may only relate to the validity of the command and not any command execution.

4.14 Flow of Overlapped Packet Commands with Data Transfer From Host to Device

This class of packet commands includes the transfer of some number of data bytes from the Host to the Device.

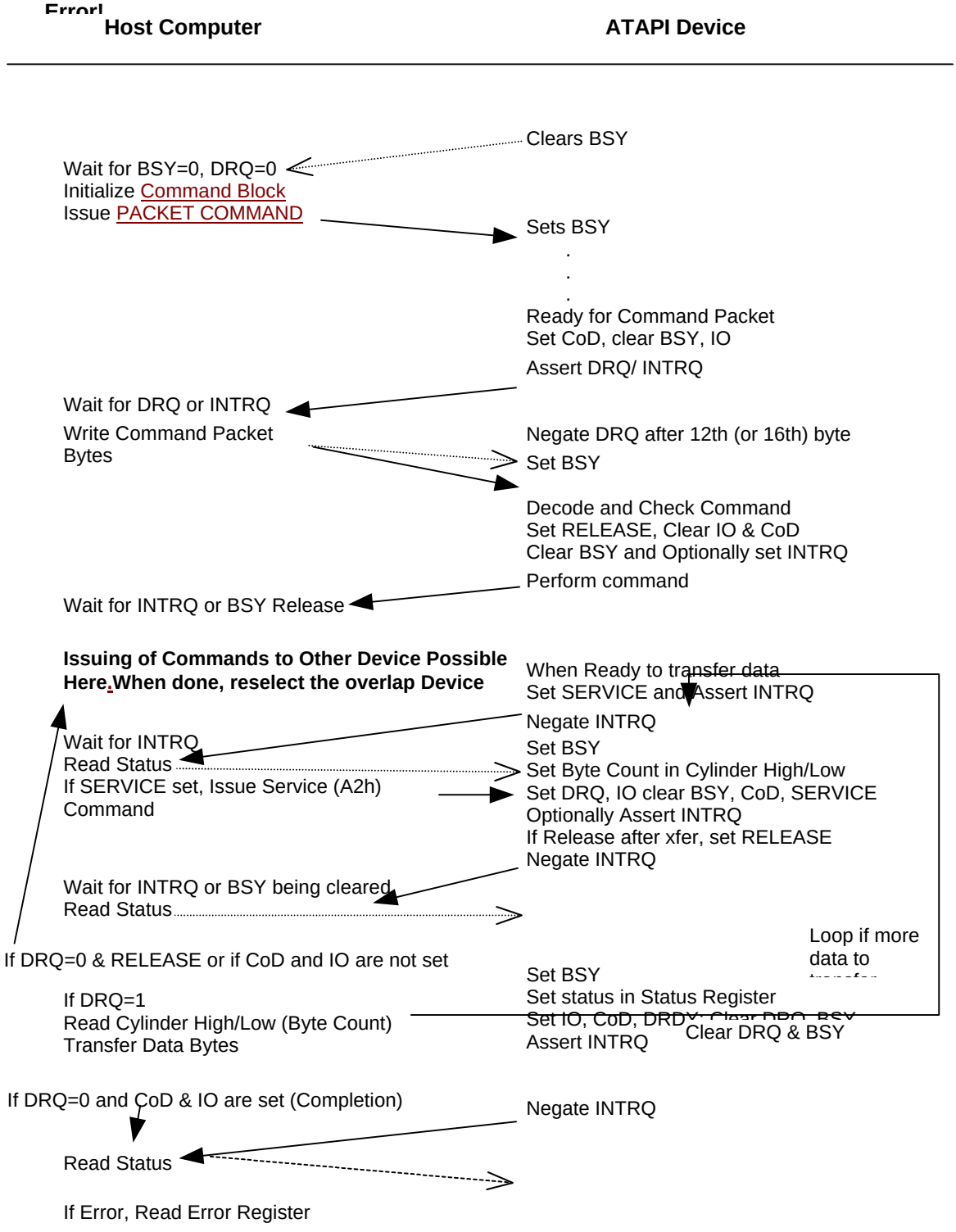
1. The host Polls for BSY=0, DRQ=0 then initializes the Command Block by writing the required parameters to the Features, Byte Count, and Drive/Head registers. The OVERLAP bit in the ATAPI FEATURES Register shall be Set to one.
2. The host writes the PACKET COMMAND code (A0h) to the Command Register and the device sets BSY to one.
3. When the Device is ready to accept the Command Packet, the Device sets C/D- and clears RELEASE, IO, BSY prior to asserting DRQ. Some Devices assert INTRQ following the assertion of DRQ.
4. After detecting DRQ, the host writes the 12 or 16 bytes of Command to the Data Register.
5. The Device(1) clears DRQ (when the 6th word is written), (2) sets BSY, (3) reads Features and Byte Count requested by the host, (4) prepares for either Release of the Bus or Data Transfer.
6. If the Device has NOT been commanded to generate an interrupt after accepting the PACKET COMMAND Data, the Device may release the Bus. In this case the device moves directly from accepting the Command Packet Data to Data Transfer (Step 12. below) with DRQ=1, C/D-=0 and IO = 0. This also be done within the time reported by the Identify Drive Data Command Data. If the Device has been commanded to generate an interrupt after processing the PACKET COMMAND, the Device shall release the Bus.
7. The Device sets the RELEASE bit in the ATAPI STATUS Register, clears IO, C/D-, DRQ, then clears BSY. If the Device has been commanded to generate an interrupt when releasing the Bus after receiving a PACKET COMMAND, the Device shall ***also*** set INTRQ pending.
8. Released State.

   At this point the Host is free to select the other Device and Issue Commands.

   Note: When the Host is Not issuing commands to the Non Overlapped Device, it should select the Overlap Device allowing it to interrupt. To promote fairness for overlapping devices which release the Bus, the host should select the overlapped device between each command issued to the non overlapped device.
9. When the Device is ready to accept data, the Device (1) sets the SERVICE Bit in the ATAPI STATUS Register, (2) sets DRQ, (3) sets INTRQ.
10. When the Device receives the SERVICE Command or if moving directly from PACKET COMMAND Data to Data Transfer, the Device (1) places the byte count of the data available into the Cylinder High and Low Registers, (2) clears SERVICE, (3) clears IO and C/D-, (4) sets DRQ and clears BSY. If the Device has been commanded to generate an interrupt when done processing the SERVICE Command, the Device shall set INTRQ (1).
11. After detecting INTRQ or that BSY has been cleared, the host reads the DRQ bit in the Status Register to determine how it proceeds with the command. If DRQ= 0 then the device has either released the Bus or terminated the command. If DRQ=1 then the host shall write the data (number of bytes specified in the Cylinder High/ Low Registers) via the Data Register. In response to the Status Register being read, the Device negates INTRQ for both cases.
12. If no more data is to be transferred, proceed to step 17.
13. The Device, leaves BSY cleared, and clears DRQ. The RELEASE Bit shall have been set at the beginning of the last data transfer. The IO and C/D- bits shall remain in the same state as for a normal data transfer. This distinguishes the “Release” from a “Status” state.

14. The above sequence is repeated from step 9.
15. The Device clears DRQ and sets BSY.
16. The Device places the completion status into the Status Register, sets C/D-, IO, DRDY, clears RELEASE, BSY, and DRQ, prior to asserting INTRQ.
17. After detecting INTRQ & DRQ=0, the host reads the Status Register and if necessary, the Error Register for the command completion status. If the Host detects that the RELEASE Bit or that both IO and C/D- are not set this is not a status state but a release state and should proceed accordingly.

The RELEASE Bit is used to signal that the Drive has released the Bus. The RELEASE Bit shall be qualified by the host with both BSY and DRQ cleared. If either BSY or DRQ is set, then the value in the RELEASE bit is undefined.



Solid Lines indicate control flow, and dotted lines are actions taken but without direct control flow change occurring. This Diagram is for Visualization only, design to text.

4.15 Figure 9 - PACKET COMMAND with PIO Data In from Host

Flow of Overlapped Packet Commands with Data Transfer From Device to Host

This class includes commands such as Inquiry, Read etc. Execution includes the transfer of some unknown number of data bytes from the Device to the host.

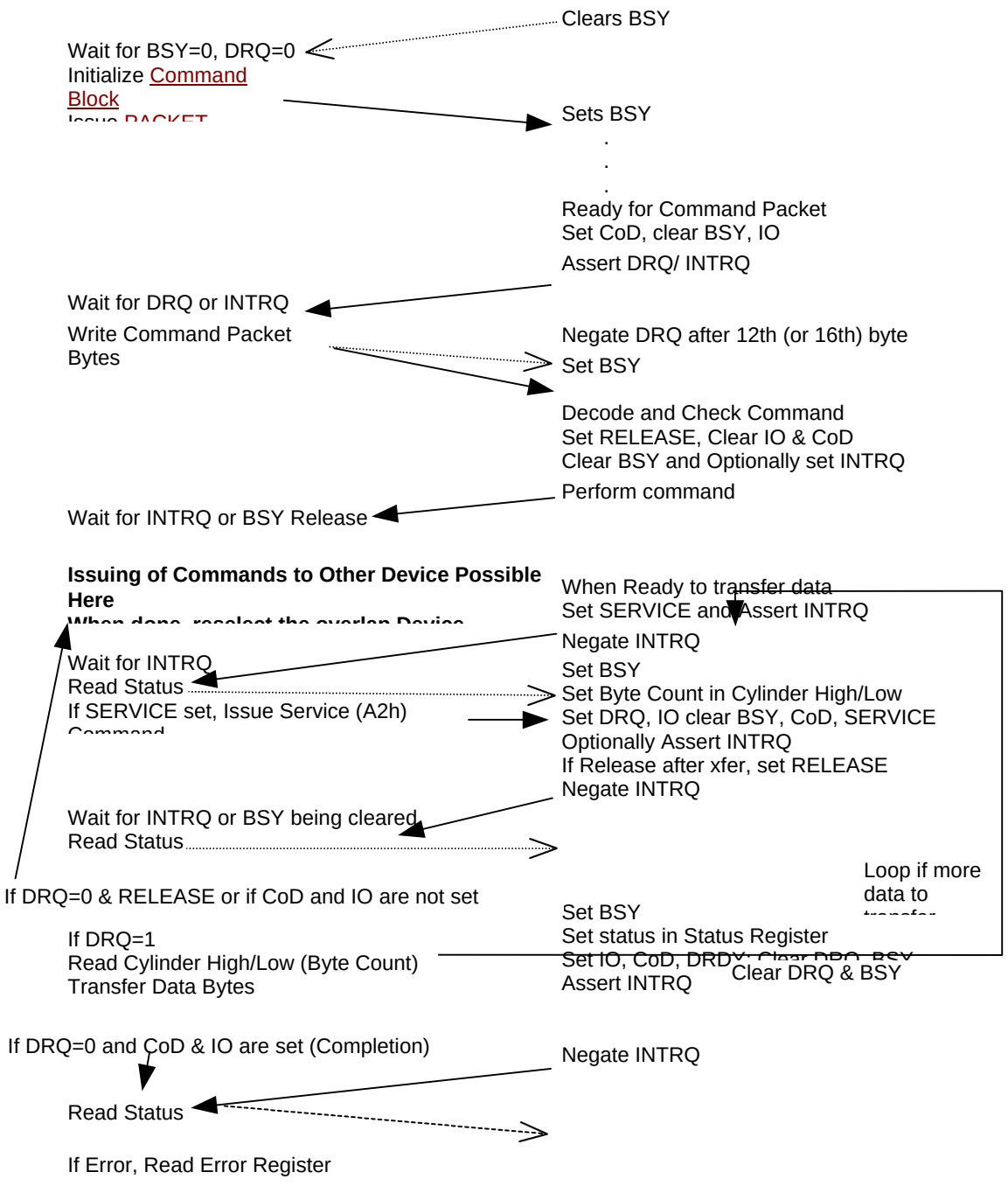
1. The host Polls for BSY=0, DRQ=0 then initializes the Command Block by writing the required parameters to the Features, Byte Count, and Drive/Head registers. The OVERLAP bit in the ATAPI FEATURES Register shall be Set to one.
2. The host writes the PACKET COMMAND code (A0h) to the Command Register.
3. The Device sets BSY, before the next Host read of the status register, and prepares for Command Packet transfer.
4. When the Device is ready to accept the Command Packet, the Device sets C/D- and clears RELEASE, IO, BSY prior to asserting DRQ. Some Devices assert INTRQ following the assertion of DRQ.
5. After detecting DRQ, the host writes the 12 or 16 bytes of Command to the Data Register.
6. The Device(1) clears DRQ (when the 6th word is written), (2) sets BSY, (3) reads Features and Byte Count requested by the host, (4) prepares for either Release of the Bus or Data Transfer.
7. If the Device has NOT been commanded to generate an interrupt after accepting the PACKET COMMAND Data, the Device may optionally not release the Bus. In this case the device shall move directly from accepting the Command Packet Data to Data Transfer (Step 12. below) with DRQ=1, C/D-=0 and IO = 0. This shall also be done within the time reported by the Identify Drive Data Command Data. If the Device has been commanded to generate an interrupt after processing the PACKET COMMAND, the Device shall always release the Bus.
8. The Device (1) sets the RELEASE bit in the ATAPI STATUS Register, (2) clears IO, C/D-, DRQ, (3) clears BSY. If the Device has been commanded to generate an interrupt when releasing the Bus after receiving a PACKET COMMAND, the Device shall ***set INTRQ (1).***
9. Released State.

   At this point the Host is free to select the other Device and Issue Commands. When the Host is Not using the Non Overlapped Device it selects the Overlap Device allowing it to interrupt.
10. When the Device is ready to accept data, the Device (1) sets the SERVICE Bit in the ATAPI STATUS Register, (2) sets DRQ, (3) sets INTRQ.
11. After detecting INTRQ, the Host shall read the ATAPI STATUS Register to determine if the selected device is requesting service. If there is an overlapped command active on the non-selected device, the Host shall change the DRV Bit and read the ATAPI STATUS Register to determine if service is also needed on the non-selected Device. When the state of both Device's SERVICE bits are known the Host shall select one of the Devices, that is requesting service, and issue the Service (A2h) Command. The Host shall employ some fairness technique in choosing which Device is serviced.
12. When the Device receives the Service Command or if moving directly from PACKET COMMAND Data to Data Transfer, the Device (1) places the byte count of the data available into the Cylinder High and Low Registers, (2) clears SERVICE, (3) clears IO and C/D-, (4) sets DRQ and clears BSY. If the Device has been commanded to generate an interrupt when done processing the Service Command, the Device shall set INTRQ (1).
13. After detecting INTRQ or that BSY has been cleared, the host reads the DRQ bit in the Status Register to determine how it proceeds with the command. If DRQ= 0 then the device has either released the Bus or terminated the command. If DRQ=1 then the host shall read the data (number of bytes specified in the Cylinder High/ Low Registers) via the Data Register. In response to the Status Register being read, the Device negates INTRQ for both cases.
14. If no more data is to be transferred, proceed to step 17.

15. The Device (1) leaves BSY cleared, (2) clears DRQ. The RELEASE Bit shall have been set at the beginning of the last data transfer. The IO and C/D- bits shall remain in the same state as for a normal data transfer, this distinguishes the “Release” from a “Status” state.
16. The above sequence is repeated from step 9.
17. The Device clears DRQ and sets BSY.
18. The Device places the completion status into the Status Register, sets C/D-, IO, DRDY, clears RELEASE, BSY, and DRQ, prior to asserting INTRQ.
19. After detecting INTRQ & DRQ=0, the host reads the Status Register and if necessary, the Error Register for the command completion status. If the Host detects that the RELEASE Bit or that both IO and C/D- are not set this is not a status state but a release state and should proceed accordingly.

The DRQ signal is used by the device to indicate when it is ready to transfer data, and is cleared after (during) the last byte of data to be transferred. This applies for both Command Packet as well as normal read/write data.

The RELEASE Bit is used to signal that the Drive has released the Bus. The RELEASE Bit shall be qualified by the host with both BSY and DRQ cleared. If either BSY or DRQ is set, then the value in the RELEASE bit is undefined.



Solid Lines indicate control flow, and dotted lines are actions taken but without direct control flow change occurring. This Diagram is for Visualization only, design to text.

Figure 10 - PACKET COMMAND with PIO Data In to Host 1112

4.16 Control Signal Timing Requirements and Relationships

The order that the signals change shall adhere to the following conditions:

1. Upon receiving the A0h ATAPI Packet Command the Device shall have BSY set until the next host access of the Status Register where the device guarantees that C/D-=1 and IO=0.
2. The Device shall not set DRQ to one until C/D- and IO are valid for the command or data packet to be transferred and the device is ready to perform that transfer.
3. DRQ may be set before or after BSY has been cleared.
4. The Device shall clear BSY and set DRQ within the time-out specified by the CMD DRQ Type.
5. Devices reporting CMD DRQ Type “Accelerated” shall clear DRQ within 5us of the last word transferred for a command or data packet.
6. Devices reporting a CMD DRQ Type other than “Accelerated” shall clear DRQ, before asserting INTRQ, following the last word transferred for a command or data packet.

Implementer’s Note: Early ATAPI Devices reporting CMD DRQ Types other than “Accelerated” may not be able to de-assert DRQ before the next INTRQ. The Host should therefore wait until the device asserts INTRQ before testing DRQ following the transfer of the last data word in a command or data packet.

5. ATAPI Transport Mechanism

The Transport Mechanism provides for the hardware support to connect the host computer to the Device.

5.1 Reset Conditions

There are three types of Reset Condition to which ATAPI Devices shall respond. In order of precidence ATAPI Devices shall respond to the following reset:

- **Power On Reset or Hardware Reset:**
- **ATAPI Soft Reset:**
- **ATA SRST:**

5.1.1 Power On or Hardware Reset

Each ATAPI Device, as it is powered on, shall perform appropriate internal reset operations, and internal test operations.

ATAPI Devices upon detection of reset, shall:

1. Clear all Commands and I/O operations in progress.
2. Return to Devices default configuration.
3. Perform the DASP / PDIAG sequence.
4. Return any ATAPI Device operating modes to their appropriate initial conditions, similar to those conditions that would be found after a normal power-on reset. MODE SELECT conditions shall be restored to their last saved values if saved values have been established. MODE SELECT conditions for which no values have been saved shall be returned to their default values.
5. Initialize the Command Block Registers as follows: Status = 00h, Error = 01h, Sector Count = 01h, Sector Number = 01h, Cylinder Low = 14h, Cylinder High =EBh and Drive/Head = 00h. A value other than 00 in the status register prior to the receipt of the first ATAPI Command Packet from the host may cause the ATAPI Device to be incorrectly identified by the host as an ATA compatible disk drive. BSY = 0, following any Reset, indicates to the Host that the registers within the Command Block have been initialized.

5.1.2 ATAPI Soft Reset Command and Protocol

ATA specifies a mandatory software reset capability because it provides a recovery mechanism from a class of errors/ problems that are recoverable in no other way. The current DEVICE drivers invoke this feature at some point in their error recovery procedures today.

The ATA software reset mechanism, SRST, (bit 2 in the Device Control Register) shall not be used for ATAPI Devices, because resets issued by the ATAPI driver would also reset any attached hard disk and vice versa.

ATAPI Soft Reset shall be detected/decoded by the interface controller circuitry.

Upon detection of the ATAPI Reset command, the device shall:

1. Set BSY. When the reset sequence in the Device is complete the BSY bit is cleared. This is the only status returned to the host by the ATAPI Soft Reset command.
2. Initialize the Command Block with the same information as after a Power On Reset. See section "5.1.1 Power On or Hardware Reset" on page 35 for a description of the initialization sequence, with the exception of the DRV bit which shall remain unchanged.

5.1.4 ATAPI Implementation of ATA SRST

It is recommended that the host not issue ATA SRTS while ATAPI commands are in progress.

To maintain Master / Slave compatibility with ATA disk drives and prevent detection of ATAPI Devices by non ATAPI-aware BIOS, ATAPI Devices shall implement the following upon receipt of an ATA SRST:

1. Follow the SRST Sequence defined in "**Error! Reference source not found.**" on page **Error! Bookmark not defined.**, and not the sequences shown in the ATA Specification.
2. Initialize the Command Block with Status = 00h or 10h, Error = 01h, Sector Count = 01h, Sector Number = 01h, Cylinder Low = 14h, Cylinder High =EBh and Drive/Head = 00h
3. The functionality of the DRDY and SERVICE bits shall be restored on the first command following an SRST.
4. Continue executing commands or play operations.
5. Leave Mode settings or Set Feature settings unchanged.
6. If a selected ATAPI Device detects SRST while its own DRQ or BSY is Set to one, then the command in progress shall be stopped.

5.2 Physical Connection

The ATAPI Devices are selected by the DEV bit in the DeviceSelect Register. When the ATAPI Device is attached along with an ATA Mass Storage Device, the ATAPI Device shall be set as Device 1 and respond as a Slave.***6***

5.4 Single Device Configurations

There may be either one or two drives attached to the ATA Bus, and thus four configurations are possible. Even though there are four possible configurations, only three of them are recommended. An ATAPI Device shall detect each of these three configurations and respond according to "Table 7 - Shadow Registers" on page 37.

There are configurations where there may be only one Master or Slave present on the Bus. In this case there is a "Shadowing" of the registers for the non-existent device. The following table shows the actions to take.

Table 7 - Shadow Registers

Jumper ->	DRV Bit	Configuration	Action
Master	0	Don't Care	Drive Bus
	1	Slave Present	Float Bus
	1	Slave Not Present	Shadow
Slave	0	Master Present	Float Bus
	0	Master Not Present	This is not a recommended Configuration. Float Bus
	1	Don't Care	Drive Bus
CSEL=M		Same as Master DRV=0	
		Same as Master DRV=1	
CSEL=S		Same as Master DRV=0	
		Same as Master DRV=1	

Table 9 - Shadowing for Single Device Configurations

Drive 0 Register Description	Drive 1 (Non-existent Slave) Use of the Register
Control Block Registers	
Alternate ATAPI Status	This may be either be a complete duplicate of the Device 0 Status (Shadowed) or Some of the bits are explicitly for Device 1 (e.g. CHECK)
Device Control	Writing to this register writes to Device 0's Device Control Register
Command Block Register	
Data	Should not be used for the non-existent slave
ATAPI Error Register	This may be either be a complete duplicate of the Device 0 ATAPI Error Register or the Register is explicitly for Device 1 (Not Shadowed)
ATAPI Features	Writing to this register writes to Device 0's ATAPI Features Register
ATAPI Interrupt Reason Register	These are an exact duplicate of Device 0's register. Implementer's Note: As the Signature is placed in these Registers, both Device 0, and the non-existent Device 1 have an "ATAPI Signature" after a reset condition. To detect that Device 1 does not exist requires a command be issued to Device 1 and detecting the Abort.
ATAPI Byte Count Register (bits 0-7)	
ATAPI Byte Count Register (bits 8-15)	
Device Select	Writing to this register writes to Device 0's Device Select Register
ATAPI Status	This may be either be a complete duplicate of the Device 0 Status (Shadowed) or Some of the bits are explicitly for Device 1 (e.g. CHECK)
ATA Command	Commands to Device 1 are aborted. Implementer's Note: The Error bit is set to abort a command to Device 1, if the Status and Alternate Status Registers are complete shadows of Device 0's Register, changing the DRV bit and reading the Status Register also show an error condition that does not exist. It is recommended that the ERROR bit not be shadowed, but a separate bit for the non-existent drive 1.

Implementer's Note: Device 0 (Master) is able to determine if Device 1 (Slave) is present, but Device 1 can't determine if Device 0 is present. Device 0 sees the Slave drive assert the DASP signal during the Reset procedure, indicating that the Slave is present.

5.5 Register Mapping

Communication to or from the Devices is through I/O Registers that route the input or output data to or from registers (selected) by a code on signals from the host (CS0-, CS1-, DA2, DA1, DA0, DIOR- and DIOW-).

5.6 Register Map PACKET / SERVICE Commands

Logic conventions are: A = signal asserted, N = signal negated, x = does not matter which it is.

Table 10 - I/O Port Functions/Selection Address (Compatibility Model)

Addresses					Functions	
CS0	CS1	DA2	DA1	DA0	Read (DIOR-)	Write (DIOW-)
					Control Block Registers	
N	A	0	0	0	Floppy A Status	Unused
N	A	0	0	1	Floppy B Status	Unused
N	A	0	1	0	Unused	Floppy Digital Output
N	A	0	1	1	Floppy ID / Tape Control	RESERVED
N	A	1	0	0	Floppy Controller Status	RESERVED
N	A	1	0	1	Floppy Data Register	
N	A	1	1	0	Alternate ATAPI Status	Device Control
N	A	1	1	1	*Note*(1)	Not Used
					Command Block Registers	
A	N	0	0	0	Data	
A	N	0	0	1	ATAPI Error Register	ATAPI Features
A	N	0	1	0	ATAPI Interrupt Reason Register	Unused
A	N	0	1	1	Reserved for SAM TAG Byte	
A	N	1	0	0	ATAPI Byte Count Register (bits 0-7)	
A	N	1	0	1	ATAPI Byte Count Register (bits 8-15)	
A	N	1	1	0	Device Select	
A	N	1	1	1	ATAPI Status	ATA Command

(1) This register is obsolete. It is recommended that a device not respond to a read of this address. If a device does not respond, it shall not drive the DDF signal.

With the exception of the Data Register, all the ATAPI registers are referenced using Byte (8 Bit) Read and Writes. The Data Register is ALWAYS referenced as a 16 bit word.

Table 11 - ATAPI Status Register (ATA Status Register)

D7	D6	D5	D4	D3	D2	D1	D0	
BSY	DRDY	DMA READY	SERVICE	DRQ	CORR	Reserved	CHECK	Read

DRDY, CORR and CHECK shall only be valid at the end of the completion of the command.

Bit 7	BSY	Busy is set whenever the drive has access to the Command Block.
Bit 6	DRDY	Indicates that the drive is capable of responding to an ATA command.
Bit 5	DMA READY	This bit indicates that the device is ready to start a DMA data transfer. It is used to communicate to the overlap capable PCI DMA logic that this service interrupt is going to transfer data via DMA. *Note that this bit is used for* Device *Fault (DF) when Overlap operation is not enabled.*
Bit 4	SERVICE	This bit signals that the device is requesting service or interrupt. It is set when the interrupt is requested and does not clear until the Service (A2h) command is issued.
Bit 3	DRQ	Data Request - Indicates that the device is ready to transfer a word or byte of data between the host and the drive. The information in the ATAPI Interrupt Reason is also valid during a Packet Command when the DRQ is set.
Bit 2	CORR	Indicates if a Correctable Error occurred.
Bit 1	Reserved	IDX in ATA, Reserved in ATAPI
Bit 0	CHECK	Indicates that an error occurred during execution of the prior previous command. The bits in the Error Register contains the sense Code.

Table 12 - ATAPI Error Register (ATA Error Register)

D7	D6	D5	D4	D3	D2	D1	D0	
ATAPI Sense Key				MCR	ABRT	EOM	ILI	Read

Bits 7-4	ATAPI Sense Key	The ATAPI sense key are defined in the device specific command standard.
Bit 3	MCR	Media Change Requested, is used and defined as in the ATA Standard.
Bit 2	ABRT	Aborted Command, is used and defined as in the ATA Standard.
Bit 1	EOM	End Of Media Detected.
Bit 0	ILI	Illegal Length Indication.

Table 13 - ATAPI Feature Register (ATA Feature Register)

D7	D6	D5	D4	D3	D2	D1	D0	
Reserved						OVERLAP	DMA	Write

Bit 7-2	Reserved	Reserved for future enhancement.
Bit 1	OVERLAP (Optional)	The device may release the BusATA bus before this command has completed. Release of the BusATA bus is at the discretion of the device.
Bit 0	DMA (Optional)	Any data for the Command is transferred via the DMA interface. Note this does not apply for the Command Packet.

Table 14 - ATAPI Byte Count Register (ATA Cylinder High/Low Register)

D7	D6	D5	D4	D3	D2	D1	D0	
Byte Count (Bits 0-7)								R/W
Byte Count (Bits 8-15)								R/W

The Byte Count is used for PIO only. The maximum count shall be set by the host prior to the issuance of the Packet Command. When any data is to be transferred, the ATAPI Device sets the Byte Count to the actual amount of data that the Host shall transfer and then issues the DRQ Interrupt. The contents of this register shall not change during the DRQ.

Table 15 - ATAPI Interrupt Reason Register (ATA Sector Count Register)

D7	D6	D5	D4	D3	D2	D1	D0	
Reserved					RELEASE	IO	C/D-	Read

Bit 7-3	Reserved	
Bit 2	RELEASE	Release indicates that the device has released the ATA Bus before completing the command in progress.
Bit 1	IO	Direction for the Information transfer, where in to the Host is indicated by a value of one and out to the device is zero.
Bit 0	C/D-	Command or Data. When this bit is zero then the information being transferred is parameter datauser data, when one then the data is Command.

Table 16 - ATAPI Interrupt Reason Register (ATA Sector Count Register)

IO	DRQ	C/D-	
0	1	1	Command - Ready to Accept Command Packet Bytes
1	1	1	Message (Future) - Ready to Send Message data to Host
1	1	0	Data To Host- Send command parameter data (e.g. Read Data) to the host
0	1	0	Data From Host - Receive command parameter data (e.g. Write Data) from the host
1	0	1	Status - Register contains Completion Status

Table 17 - ATAPI Device Select Register (ATA Drive / Head Select Register

D7	D6	D5	D4	D3	D2	D1	D0	
1	Reserved	1	DEV	Reserved for SAM LUN				R/W

Bit 7	1	Set to One for ATA compatibility.
Bit 6	Reserved	
Bit 5	1	Set to One for ATA compatibility.
Bit 4	DEV	This bit selects either Device 0 (DEV=0) or 1 (DEV=1).
Bit 3-1	Reserved	Reserved for SAM LUN

Table 18 - ATAPI Device Control Register (ATA Device Control Register)

D7	D6	D5	D4	D3	D2	D1	D0	
Reserved				1	SRST	nIEN	0	Write

Bit 7-4	Reserved	
Bit 3	1	Set to One for ATA compatibility.
Bit 2	SRST	This bit is the Software Reset. The ATAPI Device shall follow the reset sequence for SRST defined in "6.3 ATAPI Implementation of ATA SRST" on page 59. There is also a ATAPI also supports a RESET COMMAND (see "5.1.2 ATAPI Soft Reset Command and Protocol" on page 35).
Bit 1	nIEN	This bit enables/disables the interrupt to the host. When nIEN=0 and the device is selected, INTRQ shall be enabled through a tri-state buffer. When nIEN=1 or the device is not selected, the INTRQ signal shall be in a high impedance state
Bit 0	0	Cleared to Zero for ATA compatibility.

6. ATAPI IDENTIFY DEVICE Command (A1h)

The ATAPI IDENTIFY DEVICE command enables the host to receive device configuration data from the device. Configuration data is returned as a single 512 byte sector of parameter data. configuration parameter data returned by the device is is simular in format to that returned by ATA devices using the ATA IDENTIFY DEVICE command. The fields that shall be returned by the ATAPI IDENTIFY DEVICE are shown as Mandatory in the table bellow. Optional fields which are not supported by the device shall be set to zero.

The ATAPI IDENTIFY DEVICE command uses the same protocol as the ATA IDENTIFY DEVICE command with a single exception. The host may issue the ATAPI IDENTIFY DEVICE command regardless of the state of DRDY.

The device shall have data ready to transfer within 200ms of the reciept of the ATAPI IDENTIFY DEVICE command.

The table below shows only the optional and mandatory ATAPI IDENTIFY DEVICE fields. All other fields shall be returned as zero.

Word	Description	Format	Use	Fixed/Var
0	General Configuration	ATAPI	M	F
10-19	Serial Number	ATA	O	F
23-26	Firmware Revision	ATA	M	F
27-46	Model Number	ATA	M	F
49	Capabilities	ATA	M	V
51	PIO Cycle Time	ATA	M	F
52	DMA Cycle Time	ATA	M	F
53	Validity Field	ATA	M	V
62	Single Word DMA	ATA	M	V
63	Multi Word DMA	ATA	M	V
64	Advaced PIO	ATA	M	F
65	Minimum DMA Transfer Cycle Time	ATA	M	F
66	Recomended DMA Transfer Cycle Time	ATA	M	F
67	Minimum PIO Transfer Cycle Time Without Flow Control	ATA	M	F
68	Minimum PIO Transfer Cycle Time With IORDY Flow Control	ATA	M	F
71	Typical time (us) for release when processing a overlapped cmd	ATAPI	O	F
71	Typical time (us) for release after recieving the SERVICE cmd	ATAPI	O	F
73	Major Revision Number	ATA	O	F
74	Minor Revision Number	ATA	O	F
M = Mandatory, O = Optional, F = Fixed, V = Variable See ATA for definition of fields with ATA format.				

6.1 General Configuration (Word 0)

Bit Byte	7/15	6/14	5/13	4/12	3/11	2/10	1/9	0/8
0	Removable	CMD DRQ Type		Reserved			CMD Pkt Size	
1	Protocol Type		Reserved	Device Type				

Bit 15-14	Protocol Type	This field indicates the protocol used by the device. 0Xb = ATA, 10b = ATAPI, 11b = Reserved
Bit 13	Reserved	
Bit 12-8	Device Type	This field indicates the device type. (e.g. Command set used by device)
Bit 7	Removable	Indicates that device is removable.
Bit 6-5	CMD DRQ Type	This field indicates the command packet DRQ type used by the Device. 00b = Microprocessor DRQ. Device shall assert DRQ within 3ms of recieving the ATAPI PACKET Command. 01b = Interupt DRQ: device shall assert INTRQ in conjunction with the command packet DRQ within 10ms of recieving the ATAPI PACKET Command. 10b = Accelerated DRQ; Devoce shall assert DRQ within 50us or recieving the ATAPI PACKET Command. 11b = Reserved for future use.
Bit 4-2	Reserved	
Bit 1-0	Cmd Packet Size	This field indicates the size of the command packets used by this device. 00b = 12 bytes, 01b = 16 bytes, 1Xb = Reserved.

6.2 Typical Time for Release After ATAPI PACKET Command Received (Word 71)

Devices reporting support for overlap operations shall report the typical (3 sigma) time in nanoseconds that the device requires to release the ATA Bus after reciept of an ATAP PACKET Command.

6.3 Typical Time for Release After SERVICE Command Received (Word 72)

Devices reporting support for overlap operations shall report the typical (3 sigma) time in nanoseconds that the device requires to release the ATA Bus after reciept of a SERVICE Command.

7. New Set Features Commands for Overlaped Commands.

Four new SET FEATURES commands have been ADDED to enable and disable interupts for the RELEASE and SERVICE commands.

7.1 Enable RELEASE Interrupt (D5h)

A setting of 5Dh shall cause devices supporting overlapped commands to issue an interupt to the host when the device has released the ATA Bus.

7.2 Disable RELEASE Interrupt (DDh)

A setting of DDh shall cause devices supporting overlapped commands to not issue an interupt to the host when the device has released the ATA Bus.

7.3 Enable SERVICE Interrupt (5Eh)

A setting of 5Eh shall cause devices supporting overlapped commands to issue an interupt to the host when the device has finished procesing the SERVICE command.

7.4 Disable SERVICE Interrupt (DEh)

A setting of DEh shall cause devices supporting overlapped commands to not ssue an interupt to the host when the device has finished procesing the SERVICE command.

Annex A - BIOS and ATAPI Driver Compatibility

This section discusses the ATA features and functions that shall be provided by the ATA Device to allow the BIOS and driver to be content.

8.1 Reset Master/Slave Diagnostics Sequence

A Reset Master/Slave Diagnostics Sequence with a Good Status shall be provided or the BIOS shall not continue. When the ATAPI device is the slave device, and it does not respond after the Reset or Diagnostic Commands, the Master Device shall return an Error Condition to the Host Computer and all shall die.

8.2 SRST Initialization Sequence

The SRST bit in the ATAPI Device Control Register (See "Table 18 - ATAPI Device Control Register (ATA Device Control Register)"on page 43) shall NOT be used by the ATAPI Driver. Instead the ATAPI Device Driver shall reset the ATAPI Device utilizing the ATAPI Soft Reset command (see "5.1.2 ATAPI Soft Reset Command and Protocol" on page 35). Resetting the ATAPI Device using the ATA SRST would also reset any ATA hard drive attached, and if there are separate Drivers for an IDE and an ATAPI device, each driver would be resetting the others Device without the other driver being aware of the reset. ATAPI device should wait until SRST is cleared by the host before completing their SRST sequence.

After Receipt of an ATAPI Packet Command there are several differences from the ATA Specification:

A value other than 00h in the status register prior to the receipt of the first ATAPI Command Packet from the host may cause ATAPI Devices to be incorrectly identified by pre-ATAPI host BIOS as an ATA-compatible disk drive.

Initializing the Command Block upon receipt of an SRST should work since only immediate commands shall be executing when an ATA disk driver issues an SRST. To prevent interruption of ATAPI immediate commands which have not finished executing, the function of the SERVICE bit (i.e. command complete) shall be maintained. On a warm boot the BIOS and/or drivers may see a status of 00h or 10h, depending on whether or not an ATAPI immediate command completed at the same time the Host performed the WARM BOOT.

The signature placed in the Command Block following an SRST shall remain until the ATAPI device receives its first ATAPI command, i.e., the ATAPI device shall look NOT READY (DRDY=0). This shall not affect the ATAPI device drivers ability to send ATAPI commands to the ATAPI device since it is not required to wait for DRDY=1. However, it shall prevent ATA-compatible drivers, such as those performing power management, from sending commands to an ATAPI device until the ATAPI device has received its first ATAPI command: ATAPI Packet Command, ATAPI Identify Device, ATAPI Soft Reset.

ATAPI drivers wishing to use ATA power management commands shall poll DRDY and, if it is not set, they shall also look at the Cylinder registers for the ATAPI signature. If the signature is present, the ATAPI driver shall issue the ATAPI device an ATAPI command, re-enabling DRDY, before it may issue an ATA Power management command. Operating systems wishing to use a common ATA power management driver shall also be changed to perform this detection and recovery sequence, if they intend to power-manage ATAPI devices.

8.3 Special Handling of ATA Read and Identify Drive Commands

ATAPI drivers shall not issue SRST since it may corrupt the state of ATA IDE drives sharing the same Bus. Instead, ATAPI drivers shall use the ATAPI Soft RESET command to initialize an ATAPI device. Note that ATAPI commands shall not be issued to a device which has not already been identified as an ATAPI device. In order to provide ATAPI drivers with the ability to force a device to initialize its ATAPI signature (Cylinder High = EBh, Cylinder Low = 14h) without issuing an SRST, ATAPI devices shall abort the ATA

Read and Identify Drive commands and initialize the Command Block with the ATAPI signature before clearing BSY.

8.4 ATAPI aware BIOS and Driver Considerations

Pre-ATAPI BIOS shall not detect or configure ATAPI devices. Some of these BIOS are capable of configuring ATA hard disks for ATA Mode 3 IORCHDY operation. This places a special burden on ATAPI drivers to detect the presence of any ATA disk drives sharing the same port address and configure the ATAPI device for a compatible mode of operation.

Note that a special IDE port configuration driver , provided by the IDE card manufacturer, is necessary to configure the cards proprietary IDE configuration control registers. These proprietary IDE card drivers should be loaded before the ATAPI driver.

During ATAPI device detection, ATAPI device drivers or ATAPI-aware BIOS should verify that Status=00h (Not BSY, Not RDY) and that the ATAPI signature Cylinder High = EBh, Cylinder Low = 14h are present. If an ATAPI device is detected, then issue an ATAPI Identify Command to complete the ATAPI detection protocol and re-enable the Command Block (DRDY=1). If the device is ready to accept an ATA command, but no ATAPI signature is detected, then issue an ATA Read or Identify Drive command to the device to force the ATAPI device to initialize its signature. Then wait for BSY=0 and re-verify the presence of the ATAPI signature. If there is still no ATAPI signature present, do not configure the device.

ATAPI-aware BIOS and drivers should give special attention to managing configurations where ATAPI drivers share an IDE port address (Cable) with ATA IDE drives and their drivers. ATA IDE drivers frequently issue SRSTs to manage errors thereby causing ATAPI devices to clear DRDY as part of their SRST ATAPI signature initialization sequence. If the ATAPI driver already knows that the device it wishes to issue an ATAPI command to is an ATAPI device, then it need not take special action since issuing any of the ATAPI commands which do not require DRDY=1, shall restore the ATAPI device's ability to accept ATA commands. If, however, the ATAPI driver wishes to issue an ATA command to an ATAPI device which has received an SRST from an ATA IDE driver, it should issue the ATAPI device an ATAPI Soft Reset to restore the ATAPI device's ability to accept ATA commands.

Note that BIOS developed using this standard detect the presence of a Device(see "3.3 ATA Compatibility" on page 6) by using the IDENTIFY DRIVE command, but some other BIOS use configuration information from outside the IDE/ATA interface. It has also been discovered that some BIOS developed using this standard issue an ATA READ command to detect the presence of an ATA IDE drive. Therefore, the ATA READ and IDENTIFY DRIVE commands shall be aborted by non disk ATAPI Devices. It has also been discovered that some BIOS look at the status register to detect the presence of an ATA drive.

Implementer's Note: Implementers of ATAPI drivers which are intended to share a single Bus with a disk and disk driver should ensure that the device has completed any issued commands prior to changing the DRV bit.

8.5 Default Timing

ATAPI devices compatible with this specification shall support ATA mode 3 timing without requiring the host to configure the ATAPI device using any set features commands.

ATAPI devices shall revert to their default interface configuration on a Power On Reset or a Hardware Reset.

Implementer's Note: A Non-Overlapped low-speed drive, Mode 0-2, may affect Host performance when sharing the same Bus with hard disk drives capable of mode 3 or faster data transfer timing.